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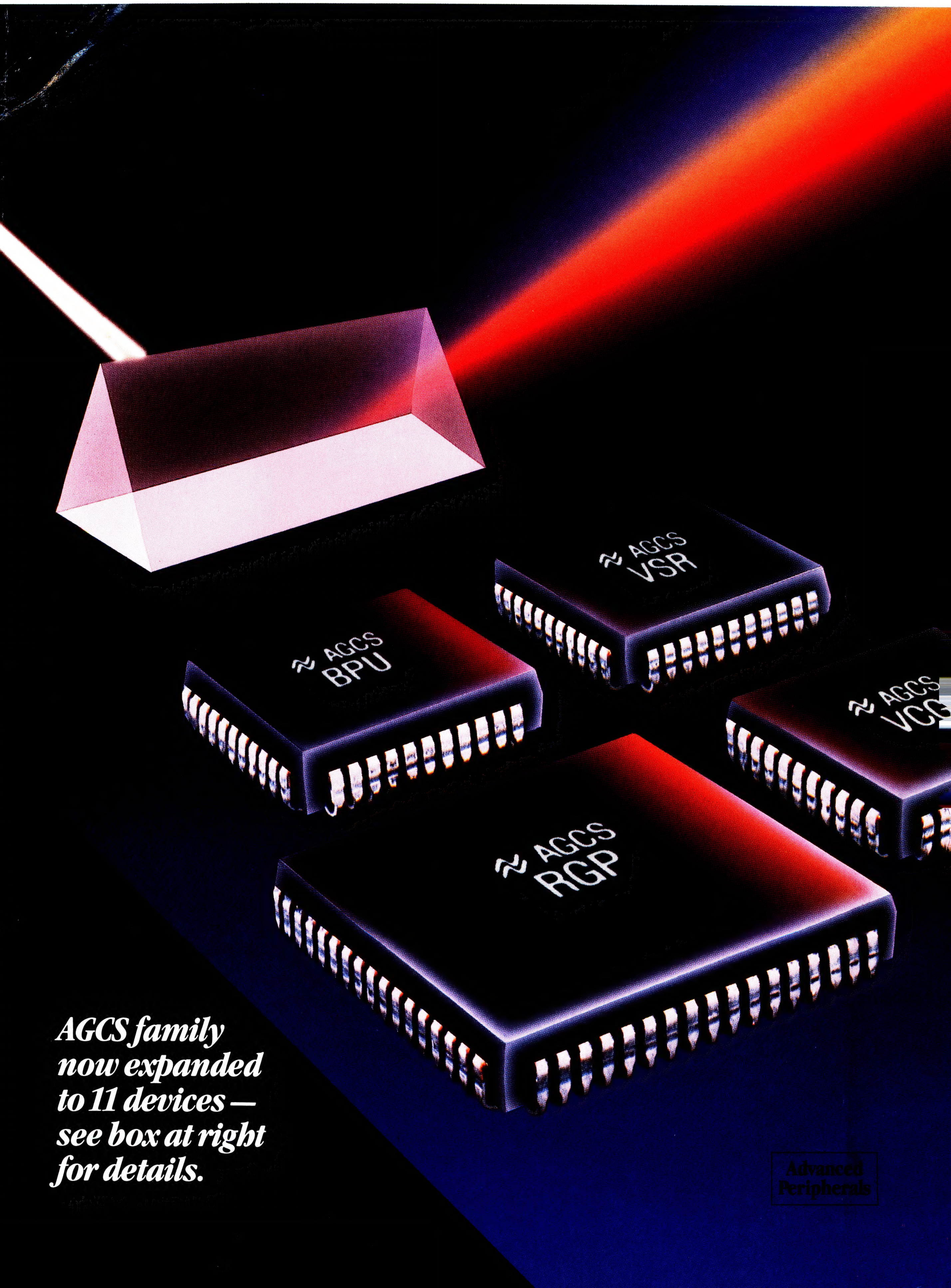

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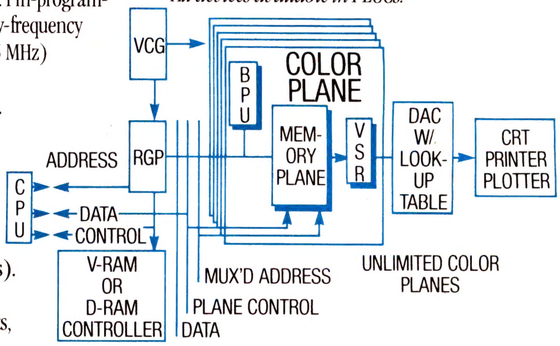

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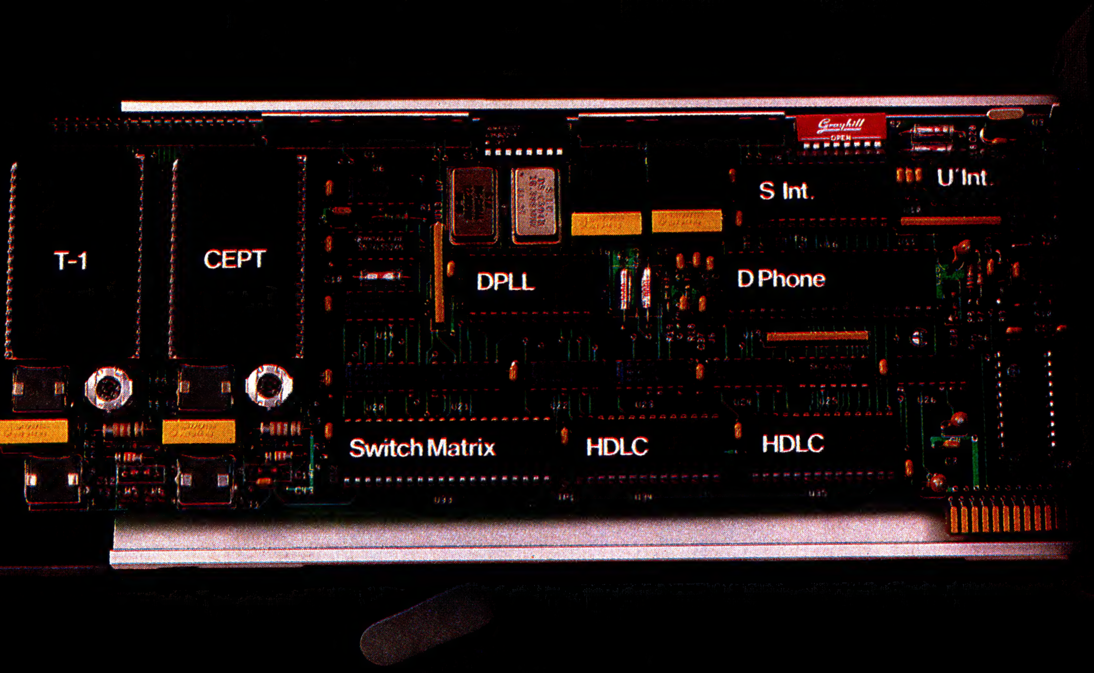

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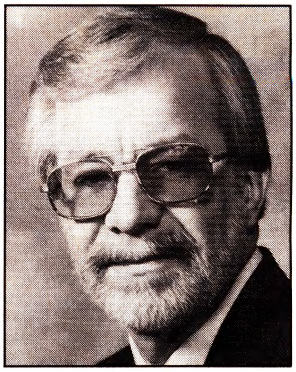

CURRAN: Keeping focused on the computer business.

Covering major stories is nothing new for Larry Curran, our Boston-based veteran who covers computers and communications developments along the East Coast. His latest contribution is the Technology to Watch on BBN Advanced Computer Inc.'s new Butterfly developments on p. 77 of this issue. In the article, he interprets how important BBN's parallel-processing architecture and new Mach 1000 operating system are to a computer industry that appears to be migrating to parallel processing for engineering and scientific applications.

Larry has spent a dozen of his 25 years in the business tracking the industry for *Electronics.* "I think my experience gives me a special perspective that's reflected in my coverage," he says. "I was in on the milestone announcements, such as Digital Equipment Corp.'s PDP-11/70 in the early 1970s and Data General Corp.'s Micronova in the mid 1970s. And from our Los Angeles bureau, I also covered Motorola Inc. in Phoenix—when it was a pioneer in emitter-coupled logic in the late 1960s and early 1970s, and ECL was supposed to take over the world."

Also while in Los Angeles, Larry was in on such major developments as ion-implantation as a new technology to boost the speed of MOS devices, and the emergence of what was then Rockwell's Autonetics division as a the first U. S. supplier of MOS calculator circuits to Japan's Sharp Corp. Those latter developments all came in the early 1970s, and Larry was on top of them from our West Coast base, where Larry Waller now holds forth. After he was transferred to Boston, where the climate seems to favor computer companies more than semiconductor firms, Curran anchored what was probably the earliest special on personal computing more than a decade ago. That opus ran in a 1976 issue—some seven years before the IBM PC turned the personal-computing world upside down.

And the beat goes on for Larry now that he is covering computers from that important hub of the industry. Since rejoining *Electronics* April 1, Larry has reported on Apollo's booming growth in work stations, Data General's plans to recover from recent setbacks, and Digital Equipment's major new MicroVAX 3500/3600 family.

He finds a special challenge in his computer beat. "Unlike semiconductor companies, computer manufacturers historically don't leak information about products in development before the ink is dry on the back-of-the-envelope design." But he believes that this guarded stance lends zest to his job as he applies the *Electronics* touch to the story he's covering: finding the unique angle, be it innovative use of semiconductors, packaging, architecture, or software, then putting it all in perspective.

Right now, he says, the computer bandwagon is rolling for reduced-instruction-set architectures. But Larry is skeptical. "I saw one sure thing, ECL, fail to win everything in sight because MOS moved so quickly. While I'm sure RISC is finding its niche, experience tells me it will face a challenging technology before long."

Laurence Altman

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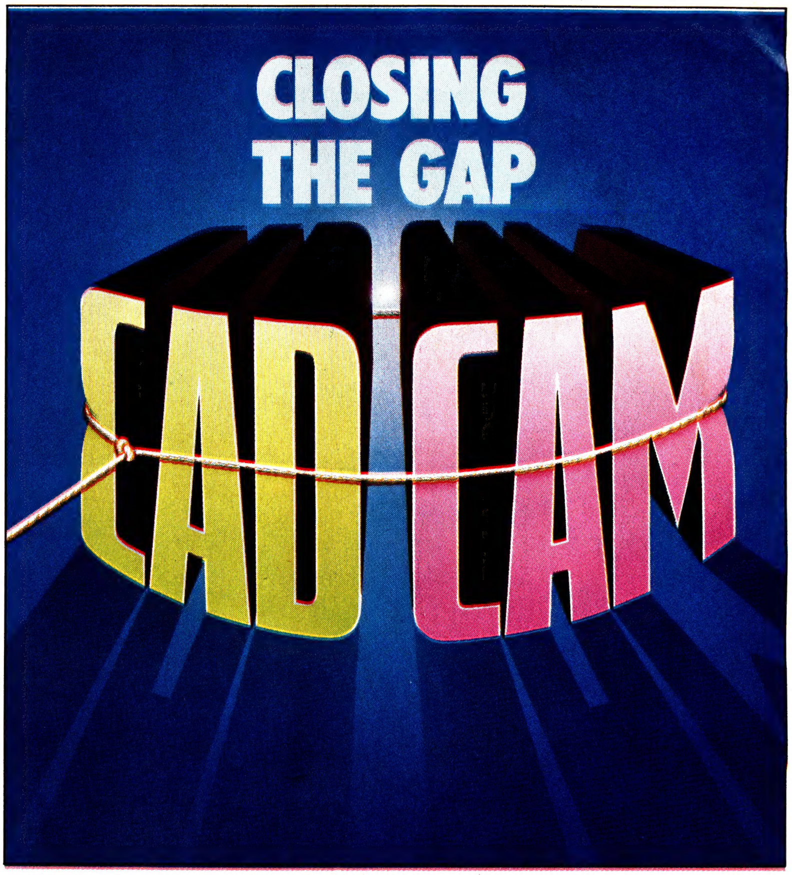

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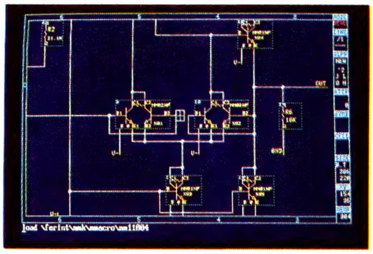
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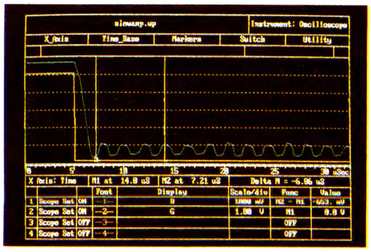

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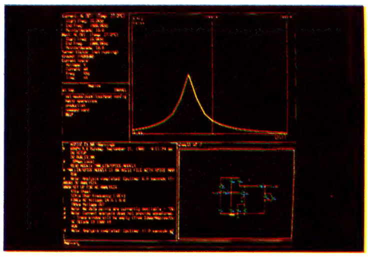
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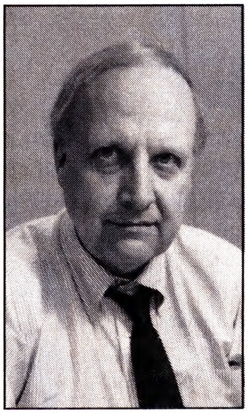
FYI

'Unfortunately, AI was just wildly oversold,' says Yale's Schank; 'we have to give it time to get beyond the expert system metaphor, which was a mistake'



So far, the technology of artificial intelligence has done a far better job of generating magazine headlines than it has of building a marketplace. AI as a business has thoroughly confused everyone from venture capitalists to corporate management, but this muddle may have reached new heights this month. Expectations have gotten way ahead of reality in expert systems, reported the Oct. 19th *Forbes*. When firms tried to use AI to build expert systems, they've come a cropper.

But just one week earlier, the Oct. 12th *Fortune* had declared: "Expert systems are now in the mainsteam computer world; companies are using them to help novices do everything from approving loans to hunting enemy submarines." Dataquest says companies will spend $250 million on software alone to develop expert systems this year, a market that will grow to $700 million by 1990. The truth lies somewhere between these two points of view.

Yes, yes, you're saying, but hasn't *Electronics* chased this same pie in the sky? Yes and no. We have written many a word on the subject of expert systems, notably in 1985 when the excitement peaked. But by a year ago, it became clear to us that problems were cropping up. We asked in an August 7, 1986, cover story: 'What's holding back expert systems?' *Forbes* estimated that investors were seduced into pouring $440 million into startup companies, yet barely 100 major expert systems have been installed.

One of the best rundowns on AI I've heard recently came from Yale professor Roger C. Schank at Technologic's fall conference in Boston: "Unfortunately, AI was just wildly oversold. It didn't get where it said it was going, because the party line was that rule-based systems and knowledge engineering was what AI was all about." He was aghast to find people thought AI could be reduced to a series of toolkits.

Part of the problem is that things move into the commercial world before they're ready, Schank says. "It's important now to give AI time to get beyond the expert-system metaphor, which was a mistake. The business world absolutely must have patience." He predicts, though, "AI is going where it was always going. We're going to make very interesting machines to talk to, and to listen to." I'm optimistic too, but I agree with *Forbes*: "the challenge for industry now is to stop dreaming of the ultimate payoff and start looking around for more opportunities closer to home."

ROBERT W. HENKEL

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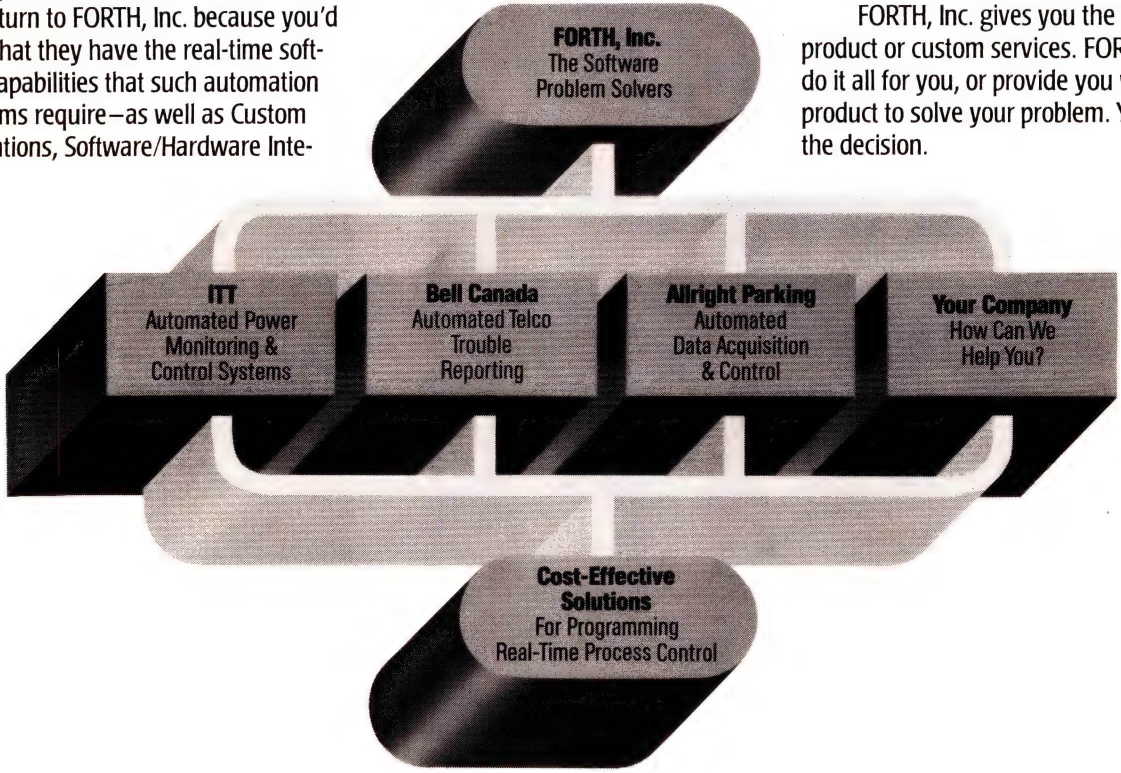

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Circle 9 on reader service card

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1 1 GHz. The 11402 Digitizing Oscilloscope features a full 1 GHz bandwidth right on the probe tip to help you make the most demanding voltage and timing measurements.

2 10-14 BIT VERTICAL/ 10 ps HORIZONTAL RESOLUTION. 10-bit vertical resolution is averageable to 14 bits. Self-calibration decreases error to less than 1% DC.

3 AUTOMATIC MEASUREMENTS. Up to six measurements can be made at the push of a button, with results simultaneously displayed and continuously updated.

4 PUSH-BUTTON HARD COPY. Plug in a Tek or compatible Epson dot matrix printer using the scopes' standard Centronics port.

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5 AUTOSET. Push a button on the front panel or on the probe to automatically set up the scope based on the signal characteristics of the selected trace.

6 TOUCH SCREEN. Select a trace, a trigger, a measurement or other function by touching the appropriate area of the screen or by selecting from pop-up menus: the closest, most natural link yet between user and scope.

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Tektronix 11402 DIGITIZING OSCILLOSCOPE
Tektronix 11401 DIGITIZING OSCILLOSCOPE

Tektronix introduces the 11000 Series: the new standard in digitizing and analog oscilloscopes.

These new fully programmable scopes display more traces (up to 8) at higher bandwidths (up to 1 GHz), with greater accuracy (up to 0.6% vertical), and include more new functions for expediting the capture and processing of data than can ever be listed here.

Two new digitizing scopes exert the power of three 16-bit processors, long records, the most powerful triggering and the highest throughput ever. Use their built-in dual timebases to easily acquire pre- or post-trigger details of a trace, and view both the whole trace and the details on screen at once.

Two analog scopes feature an integrated 500 MHz universal counter/timer for unequaled resolution, accuracy, and scope versatility— for the

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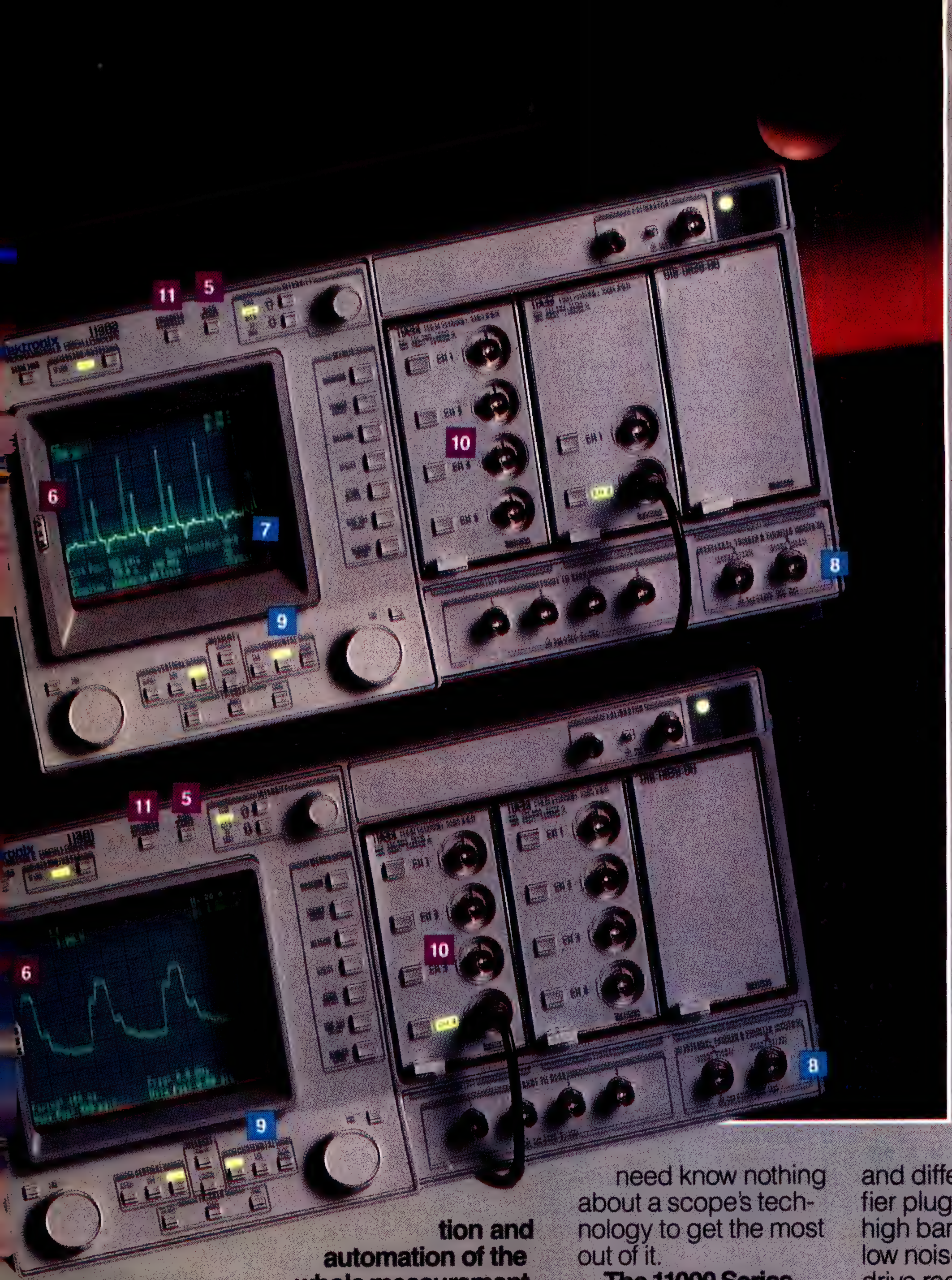

ANALOG

7 MICROCHANNEL PLATE. The single shot trace brightness of the Tek 11302 is almost 1000 times brighter than conventional scopes—enough to expose even the fastest transients to view.

8 500 MHz INTEGRATED COUNTER/TIMER. Use with dual delayed sweeps for precise timing measurements between selected points. Unique counter view trace lets you see exactly what you are triggering on.

9 CURSORS. Use to make precise measurements on any part of a displayed waveform.

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10 1 mV/DIV SENSITIVITY. Achievable from four new plug-ins. These amplifiers feature fast overdrive recovery and wide dynamic range.

11 SELF-CALIBRATION. Push the Enhanced Accuracy button to calibrate the scope from amplifier input to CRT graticule, automatically, for the best vertical accuracy available in a scope today.

price of a scope alone. A unique counter view trace lets you see exactly what you are triggering on, for a sense of confidence no conventional counter/timer can offer.

Perhaps most startling is the simplification and automation of the whole measurement and analysis process. Larger displays, pop-up and touch-screen menus, plus automated setup and measurement capabilities help unclutter the front panel and keep eyes focused on the display. For the first time, users need know nothing about a scope's technology to get the most out of it.

The 11000 Series continues the plug-in versatility of the Tek 7000 Series. Five new plug-ins and three new probes tailor the new scopes to a full range of applications, from design and debug to production test. New single-ended amplifier and differential amplifier plug-ins combine high bandwidth with low noise and fast overdrive recovery.

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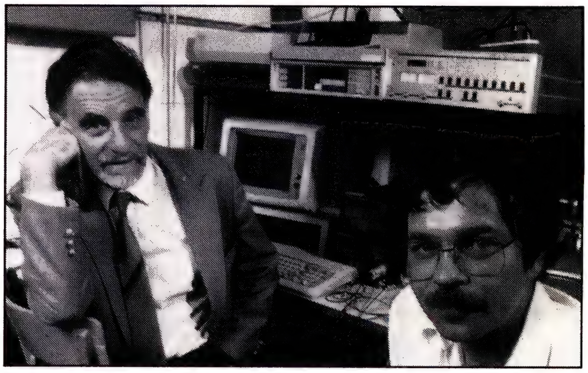
SEE PAGES 46-47 FOR DETAILS

PEOPLE

WHO'D HAVE PICKED THEM FOR A NOBEL A YEAR AGO?



LAUREATES. Mueller, left, and Bednorz are the second IBM pair to win the Nobel Prize for Physics in as many years.

NEW YORK

If anyone had suggested a year ago that the 1987 Nobel Prize for Physics would go to two men studying high-temperature superconductivity, the very idea would have drawn blank stares. But what a difference a year makes—just ask J. Georg Bednorz and K. Alex Mueller, the 1987 winners.

In 1986 superconductivity was a stalled technology, an obscure area of physics that hadn't enjoyed a major advance in a dozen years. But then the two IBM Corp. physicists, who had been studying a group of ceramic materials in their Zurich labs for almost three years, discovered that the oxides were superconductors. Overnight, it changed their world.

Ironically, the two laureates have spent most of their careers working in other fields. They only recently turned their attention to superconductivity.

Both Bednorz, 37, and Mueller, 60, earned doctorates from the Swiss Federal Institute of Technology. Neither has worked in industry anywhere but at IBM. Mueller has become well-known during his 23 years at IBM, but Bednorz is a comparative newcomer. Their close collaboration began in 1985, when Mueller decided to devote his undivided attention to superconductivity research. Together they made one of the most important discoveries the physics community had seen in decades.

Bednorz and Mueller found that the materials, oxides of copper, lanthanum, strontium, and barium, became superconductive at record high temperatures. They pushed the ceiling, then 23 K, to over 35 K. That set off a flurry of activity as researchers the world over raced to verify and improve upon the work begun in Zurich. Record highs climbed up the Kelvin scale, and within six months, claims of superconductivity at 90 K and higher were routine. "We broke an enormous psychological barrier," says Mueller.

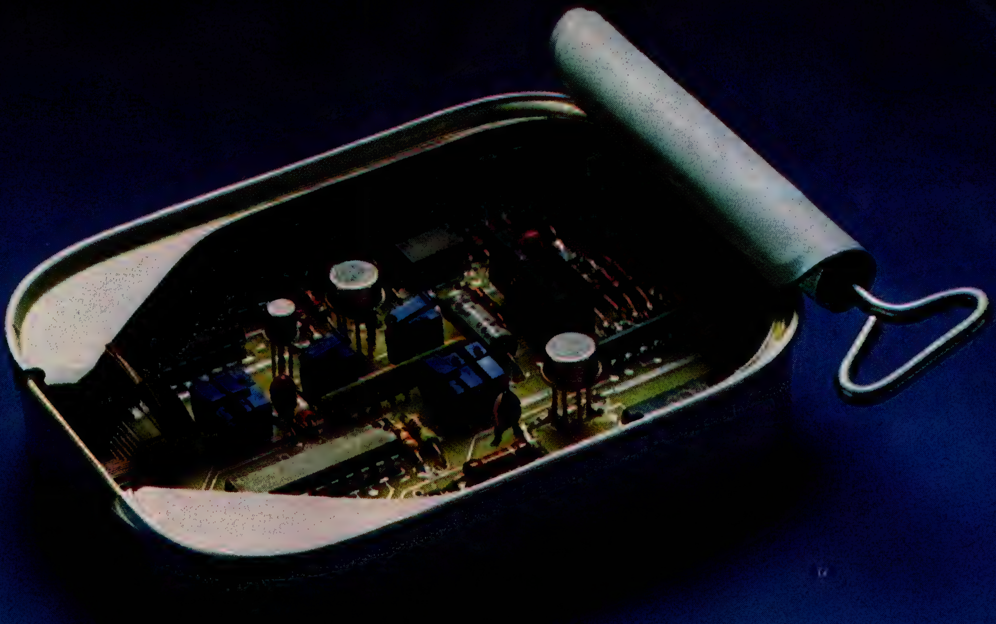
Mueller is an IBM Fellow, one of only about two dozen in the company's four research labs worldwide, and as such has free rein to work on projects of his choice at his own pace. That freedom allowed the Mueller-Bednorz collaboration to pursue a seemingly bizarre course, says Paul Horn, manager of statistical mechanics at IBM's Thomas J. Watson Research Center in Yorktown Heights, N. Y. Horn is closely involved with the ongoing superconductivity research at the Watson center. "Nobody could have predicted this [development]," Horn says. "It's only because [Mueller] had the complete freedom to go off in a direction that only Alex would have chosen."

Almost as stunning as the speed of the developments was the speed with which the Royal Swedish Academy of Sciences in Stockholm granted the award, which was announced on Oct. 14. Scientists often wait years before being recognized for their work. Last year's winners, for example, Gerd Binnig and Heinrich Rohrer, who also work at IBM's Zurich labs, waited five years after they invented the scanning tunneling microscope.

But the enormity of the superconductivity breakthrough had many insiders wondering whether Bednorz and Mueller would get the award this year. "I think it's extraordinary that we got the prize so short after our discovery," Mueller says. But Bednorz says he is more relieved than surprised. "My reaction is like, we knew about the speculation and now it's over," he says. "The tension is gone."

Bednorz, who joined IBM just five years ago, says he plans to use some of his half of the $350,000 prize "to try to buy a house." Mueller, who has spent 24 years with IBM, working in both the U. S. and Switzerland, says, "I already have a house—but I have a mortgage, too."

Both also say their superconductivity work is far from over. Tough problems remain: for example, can the brittle ceramics be made into wire? "It's like making a wire out of a toilet bowl," says Horn. *–Tobias Naegele*



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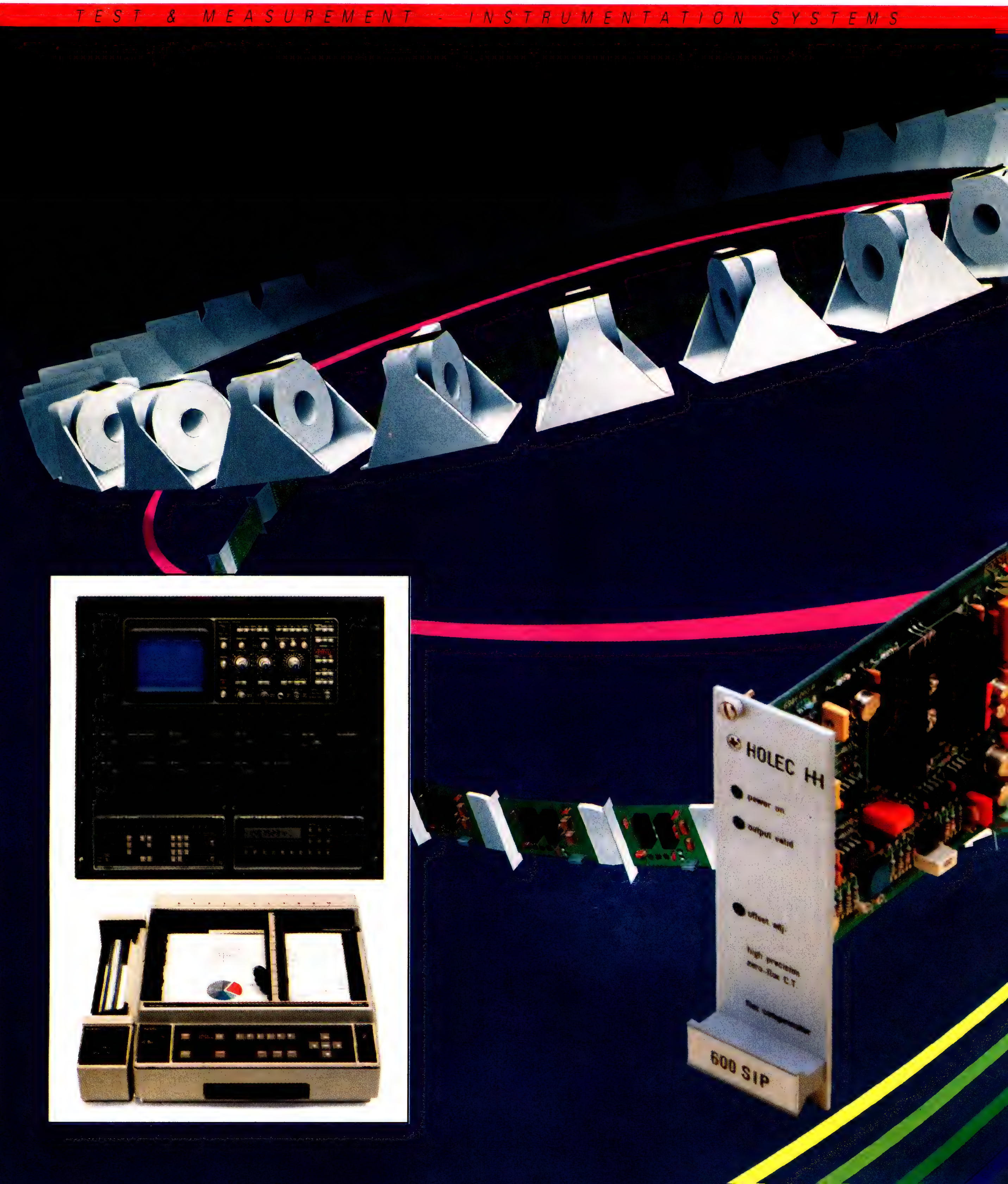

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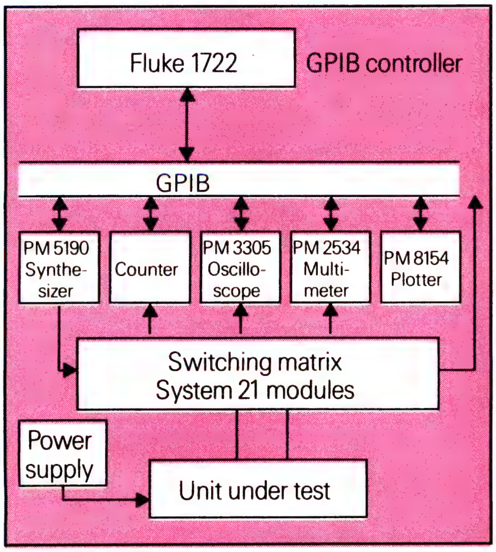
Universal System Testing

Problem. A major order for high performance, high precision DCCTs (Direct Current – Current Transformer) called for 100% functional checking of each PCB-based unit. However, the test and measurement set-up should not become redundant once the order had been completed.

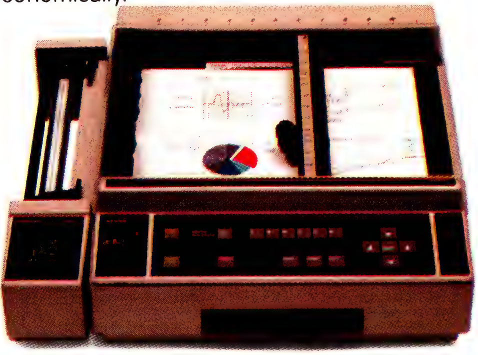
Analysis. Essentially, the DCCT is a 600A to 65kA pulsatory current meter with a accuracy of +/– 5ppm. The order (575 units) was for current control of the LEP (Large Electron Positron) at the European Laboratory of Particle Physics, CERN, in Geneva.

Our customer, Holec – one of the world's leading manufacturers of computerized control equipment for high energy applications, developed a CAT (Computer Aided Testing) system in which a hierarchal instrument controller communicates with a lower-level measurement sub-system via a GPIB-interface. Measurement protocols stored in the controller provide a library of selectable measurement cycles.

Action. Using instruments from its comprehensive Test & Measurement programme, Philips configured the lower-level sub-system with: a **PM 5190** synthesizer; a **PM 3305** DSO with **PM 8154** plotter; a **PM 2534** DMM; and a switching matrix comprising 18 **System 21** modules (12 universal switches, 2 coaxial switches, 2 user adapter units and 2 master units).



Evaluation. Holec's CAT-system can now perform up to 112 measurements per cycle. Each of 32 measurement points on the PCB under test are accessible for 3 instruments. It also has 16 channels available for random measurements.
And being a fully automated test routine, once the PCB is connected to the CAT system all measurements are performed qualitively, quantitively and economically.



Most important, when the sub-system is no longer needed for PCB testing, it can easily be reconfigured for other test purposes.

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Circle 16 on reader service card

Electronics targets military electronics in November.

In the November 26th issue, *Electronics* mobilizes its forces to examine the Microwave/Millimeter-Wave IC (MIMIC) Program.

And they'll be battling questions like: What will MIMIC do for GaAs? Which companies will be front-line contenders for the $500 million government program? And what strategies will they be using as they arm themselves for the first definition and development phase.

In addition, our editors will also take an in-depth look at new military technology advances and their impact on the commercial sector.

It's an issue of such importance that readers will fight to read it. And an issue that advertisers targeting the military electronics market will want to include as an important part of their advertising program.

It promises to be a special issue that commands attention. Don't miss it!

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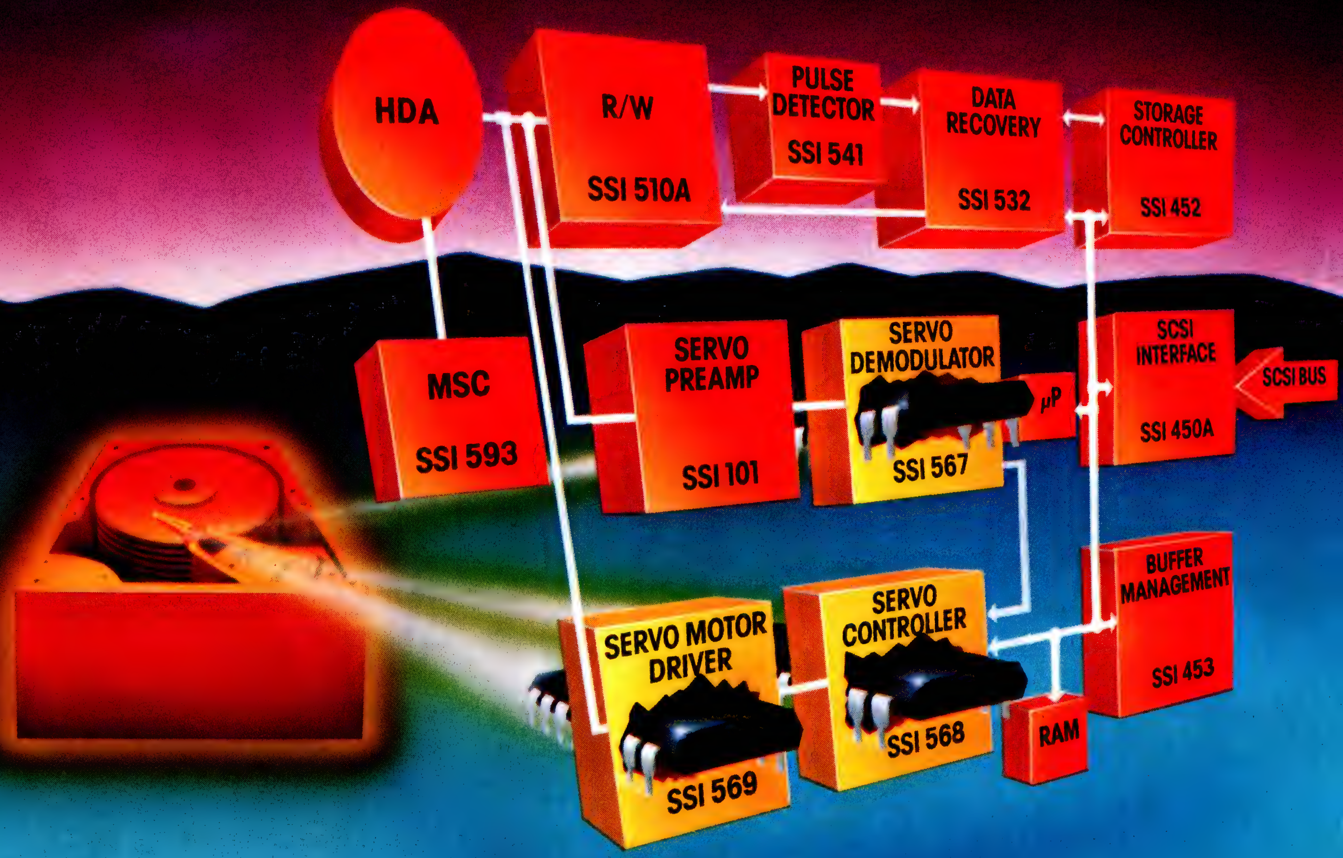
Electronics

NEW FROM SILICON SYSTEMS A SERVO CHIP SET FOR HIGH PERFORMANCE HDD's!



Silicon Systems now introduces the SSI Servo Chip Set. It is a 3-chip servo set for precise head positioning in the new high-performance hard disk drives. This is just the latest development in the company's program for the full integration of disk drive electronics.

The new set consists of the SSI 567 Servo Demodulator, which provides servo demodulation for dedicated-surface servo systems; the SSI 568 Servo Controller, which provides servo control; and the SSI 569 Servo Motor Driver, which is a voice coil servo motor predriver that is compatible with complementary power FETS. The chip set includes all the functional building blocks required in the servo channel, and is easily controlled via the microprocessor interface.

This chip set will break down major barriers to entry into the development of high performance hard disk drives. With its high level of integration, it provides superior performance and features for lower power, reduced board space, and lower cost.

For more information on the new SSI Servo Chip Set and the other exciting product families in the complete ESDI and SCSI Chip Sets for HDD and FDD disk drive electronics, contact Silicon Systems today.

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ELECTRONICS NEWSLETTER

INTEL'S 80386 OUTDOES MOTOROLA'S 68020 IN HEAD-TO-HEAD TESTS . . .

A benchmark study pitting the two leading 32-bit microprocessors—Motorola Inc.'s 68020 and Intel Corp.'s 80386—has shown the 386 to be "consistently faster than the 68020," says Elizabeth D. Rather, president of Forth Inc., of Manhattan Beach, Calif. Rather's firm supplies polyForth operating systems for both chips, as well as other processors. The head-to-head test compared similarly configured 16-MHz parts, each with cache memory and a polyForth program. The benchmark ran extensive tests that exercised all functions, Rather says. One measurement, a set of 10,000 multipy/divides, for example, showed the 386 to require only 156 ms compared to 244 ms for the Motorola chip. Rather says the results are surprising because, until the tests were completed, "we all thought the 68020 was faster." ☐

. . . AS THE LATEST 32-BIT MICROPROCESSORS HIT THE STREET

Get ready for the second-generation 32-bit microprocessors. Motorola Inc. and National Semiconductor Corp. are expected to unveil their newest entries before the end of October. Motorola's 68030 will officially bow in New York Oct. 29, but the company is already taking orders for volume shipments. The price will be about $400 for a 16.7-MHz 68030 and $550 for a 20-MHz version in unit quantities. The chip is twice as fast as its predecessor, the 68020, and boasts additional on-chip cache, integrated memory management, and increased parallel functions. NCR, Apple Computer, Unisys, and Sun Microsystems are all expected to use the new part. National, meanwhile, is just beginning to ship samples of its 32532, which adds on-chip data, an instruction cache, and memory management to the core of the existing 32032. A 20-MHz version is due in the first quarter of 1988, and a 30-MHz version will follow later. ☐

APOLLO'S NEW SERVER LOCKS OUT USERS THAT DON'T HAVE 'KEYS'

Apollo Computer Inc. is touting a more effective way to license and administer software usage on networks and will begin shipping the system, called Network License Server, in March. With NLS, software vendors license their programs with the condition that only a preset number of people will have access at any one time. Once the software is installed, it is guarded by a "lock" for which there is a limited number of "keys," limiting the number of concurrent users. NLS provides logs that monitor the use of application packages, giving license administrators better control over requests for licenses. NLS will work initially only on Apollo work stations, but will eventually run on Digital Equipment and Sun Microsystems machines. A 50-key NLS will carry a one-time charge of $4,000 or an annual fee of $1,000. The software-lock license carries a one-time charge of $5,000. ☐

AIR FORCE ORDERED TO REWRITE RFP, BUT IT CAN SPECIFY UNIX V

The Air Force was within its rights in specifying the use of AT&T Co.'s Unix System V when it sought bids for a planned order of 20,000 mid-size computers, says the General Sevices Administration Board of Contract Appeals. Digital Equipment Corp. and Wang Laboratories Inc. had filed suit against the Air Force, claiming that its request for proposals unfairly favored AT&T and other supporters of its System V Interface Definition. The appeals board didn't let the Air Force off completely, however. It ordered the RFP rewritten to eliminate "ambiguities and bias" resulting from the use of a proprietary AT&T test program. DEC will now adopt a wait-and-see posture, a spokesman says: "Whether we can go ahead with our bid and be competitive depends on the how the Air Force implements the decision." ☐

OCTOBER 29, 1987

ELECTRONICS NEWSLETTER

MAXIMUM STORAGE'S 5¼-in. OPTICAL WORM DRIVE IS FASTER

Maximum Storage Inc., a year-old optical-disk-drive maker, is moving fast to up the ante in 5¼-in. write-once, read-many-times, or WORM, drives. The firm plans to begin shipments in January on the APX-4000, a 500-Mbyte drive that more than doubles the density of its original APX-3000 product, introduced in September. The APX-4000 won't be the highest-density 5¼-in. WORM drive on the market—Maxtor Corp. offers the RXT-800S, an 800-Mbyte WORM drive made by Ricoh Co. of Japan—but the new unit will be the fastest, says Maximum. It will feature a 5-Mbit/s data-transfer rate, an average access time of 135 ms, and track-to-track speed of 1 ms. That compares to 2 Mbits/s, 168 ms, and 3 ms, respectively, for Maxtor's product. The Maximum drive will initially come with software for plug-and-play compatibility with DOS-based personal computers. In the first quarter of 1988, new software will allow it to also run on Unix-based systems; compatibility with Digital Equipment Corp.'s VMS operating system is also planned for 1988. ☐

NEURAL-NET SOFTWARE LEARNS TO RECOGNIZE PATTERNS—BY ITSELF

Unsupervised pattern learning for such jobs as image-recognition security and robotic sorting can now be implemented in adaptive resonance neural networks: Hecht-Nielsen Neurocomputer Corp. claims its AR/NET software is the first fully functional product of this type. The software works with the San Diego, Calif., company's Anza neuro-computing coprocessor system, an add-on to IBM Corp.'s PC ATs and compatibles. The network can be called as a subroutine from a program written in C. Thanks to its massively parallel nature, it recognizes a learned pattern immediately, regardless of the number of patterns stored. It does not slow down as it learns more patterns, and it can be set to signal the user when it encounters a pattern it doesn't recognize. Users can change the amount of error the program will tolerate in matching a pattern to a learned category. Owners of Anza systems can purchase AR/NET now for $495. ☐

VERBATIM CLOSES IN ON AN ERASABLE 3½-in. OPTICAL-DISK DRIVE

Verbatim Corp. is nearing the final stages of development on a 3½-in. erasable optical-disk drive. The system could debut as early as mid-1988, but is probably 12 to 24 months from full commercial production, says a Verbatim product manager. The half-height drive, which is based on thermo-magneto-optical-memory technology, will be offered as a more reliable and permanent alternative to rigid Winchester disk drives. Verbatim, a subsidiary of the Eastman Kodak Co. of Rochester, N.Y., isn't discussing the future product openly yet, but one executive promises that the drive will offer a capacity of about 50 Mbytes, access time of about 70 ms, and a data-transfer rate of 1 Mbyte/s. ☐

INTEL PLANS TWO-CHIP SET FOR 32-BIT EMBEDDED CONTROL

Intel Corp. is readying a two-chip 32-bit microcontroller for data-handling applications for introduction next spring. A 32-bit 80376 core and a companion device for expanded controller interface will maintain compatibility with Intel's current 16-bit 80186, which is aimed at data-handling duties. Intel executives hint that they will later add a 32-bit microcontroller for event-control timing applications. This would be compatible with the 16-bit 8096. Intel's plans to extend its embedded-controller line to the 32-bit level comes just as the market for 16-bit microcontrollers is emerging. Intel hopes 32-bit compatibility with its two 16-bit offerings will give it a jump on the competition when this market emerges. ☐

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By: Joe Zimmerman, Sports Staff
Marlboro, MA

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PRODUCTS NEWSLETTER

NEC'S CACHE-CONTROLLER CHIPS CAN RUN 32 GIGABYTES . . .

A cache-controller chip from NEC Corp. that handles up to 128 Kbytes of memory can be cascaded—a feature competitors *don't* offer. The theoretical limit is 250 cascaded chips controlling 32 gigabytes. Also, other cache controllers work only with a target processor—Intel Corp.'s 80386, for example—but the IC from the Tokyo-based Microcomputer Products Division supports competitors' 16- and 32-bit processors as well as its own V-Series chips. For cache memory of 32 Kbytes or larger, hit rate is 97% or higher. The chip offers a selection of cache-search algorithms: direct mapping, two-way associative, and four-way associative. Implemented in 1.2 µm CMOS, the µPD7164 will be offered in sample quantities in December and go into production in April. Sample price in Japan is 40,000 yen each. U. S. introduction is set for November, but pricing is not available. ☐

. . . WHILE TI'S CACHE-TAG CHIP WORKS WITH THE 68030 AT 40 MHz

Built to run with the 32-bit MC68030 microprocessor from Motorola Inc., Texas Instruments Inc.'s ACT2155 cache-address comparator and data random-access memory features a fast 2-bit counter and bus-interrupt interfaces that keep up with the 68030 at its announced 20-MHz speed—and up to the possible 40MHz of the future. The 1-µm CMOS chip uses its counter to generate the next addresses for internal cache storage during burst-fill mode, and the extra interface logic lets slower static RAMs serve the processor, says the Dallas company. A 2155 rated for 25-ns access easily supports a 20-MHz 68030; and an 18-ns 2155 supports 40-MHz speeds. Cache tags that are more generic would have to be 7 to 10 ns faster than this, and since the TI part favors no specific caching scheme, memory designers have more freedom than with a highly integrated controller, such as NEC's µmPD7164. The 44-pin device sells for $22.50 each. ☐

AST'S PC RUNS LIKE A PS/2 BUT USES AT-COMPATIBLE BOARDS

AST Research Inc. is bidding to steal some of the thunder of IBM's Personal System/2 with a multitasking 20-MHz machine that offers PS/2-like performance but works with the vast base of add-on boards and hardware for IBM's Personal Computer AT. Based on Intel Corp.'s 80386 microprocessor, the Premium/386 uses an arbitrated bus architecture called Smartslot that provides minicomputer capabilities by accommodating multiple coprocessors. Smartslot has three buses: a 32-bit pathway from processor to memory, a feature bus, and an arbitration bus for efficient management of memory and peripherals. Available in January, the Irvine, Calif., company's Premium/386 comes in four models, priced between $4,695 and $8,995. ☐

AI SOFTWARE DIGS NEW KNOWLEDGE OUT OF LARGE DATA BASES

Software is now at hand that leverages statistical techniques with artificial intelligence to extract knowledge from large data bases. Called IXL: The Machine Learning System, the package analyzes data in dBase III, Lotus, and ASCII formats for hidden knowledge and then formulates simple rules to illustrate the previously unknown relationships, says its maker, IntelligenceWare Inc. of Los Angeles. Running on IBM Corp. Personal Computers and compatibles, IXL handles inexact or incomplete data, and users can specify a level of acceptable error. It does not require preprogramming to analyze a data base. Instead, it accepts defined concepts—such as "large company" or "Pacific Region"—that direct the analysis toward the type of information sought. The $490 program, available now, can process large data bases overnight, allowing users to collect its results in the morning. ☐

PRODUCTS NEWSLETTER

ALLIANT'S FX/4 GIVES MINISUPERCOMPUTING A MODULAR GROWTH PATH

Users of parallel vector-processor minisupercomputers can now start small and grow, thanks to the modularity of Alliant Computer Systems Inc.'s FX/4. In a one-processor configuration, this minisupercomputer sells for $99,900—well below the $600,000 price tag of the Littleton, Mass., company's high-end FX/8 machine. But it can be expanded to a four-processor system that achieves peak 64-bit performance of 47.2 million floating-point operations/s and costs $250,000. The new processor incorporates 8,000-gate CMOS arrays and Alliant's first use of surface-mount packaging, both of which contribute to the lower cost. Alliant is also offering the FX/C compiler and algorithm advances to make the FX/4 attractive for scientific and engineering applications such as finite element analysis. ☐

DATA RACE'S PC-AT MODEM CARDS ARE OBSOLESCENCE INSURANCE

System integrators can now build the data-transmission needs of the future into their clones of the IBM Corp. Personal Computer AT with Data Race Inc.'s modem boards that cover the 300- to 9,600-baud spectrum. The PC-Race series supports two separate daughter cards—one for 9,600-baud speed (for both block-mode file transfer or interactive modes), and another for speeds of 2,400, 1,200, and 300 baud. What's more, the San Antonio, Texas, company's modems can be upgraded to higher speeds simply by adding daughter cards. Available now, a fully loaded PC-Race modem board sells for $995. The 9,600-baud daughter card sells for $795, and 300- to 2,400-baud cards are available for $595. The modems boast error-correction, full-duplex transmissions, and auto-dialing. The 9,600-baud system embodies Data Race's patented asymmetrical full-duplex, intelligent data-compression and error-correcting technology. ☐

OPTOTECH IS FIRST TO OFFER A 'JUKEBOX' FOR 5¼-in. OPTICAL DISKS

Optotech Inc. is bringing the large-capacity jukebox to 5¼-in. optical-disk storage. The Colorado Springs, Colo., company's Laserbank cartridge changer can hold up to 66 cartridges—each containing one 5¼-in. disk—and up to four disk drives. The system is compatible with Apple Computer's Macintosh, Digital Equipment's VAX family, Sun Microsystems' work stations, and IBM's Personal Computer and Personal System/2 families. The jukebox will come with all the software needed to drive any or all of these systems, so that multiple systems of different makes can share the same files. With one double-sided disk drive and the changer, the system sells for just under $10,000—about the same price as a single 12-in. optical-disk drive. Using double-sided disks with a capacity of 200 Mbytes per side yields 26.4 gigabytes of storage. ☐

WRITING SOFTWARE FOR PARALLEL-PROCESSOR CHIPS JUST GOT EASIER

Developers of software for single-instruction, multiple-data (SIMD) parallel-processor chips can cut months off the development cycle for applications such as artificial vision systems with NCR Corp.'s SIMD Processor Development System. Until now, designers had to build the controller card that directs the operation of the company's geometric arithmetic parallel-processor (GAPP) chips and coordinates timing with other hardware. But that board is supplied with the new system, which runs on an IBM Corp. Personal Computer AT. Also offered are up to four GAPP array cards, a high-speed host-interface card, and an optional frame grabber. The system comes with NCR's GAPP algorithm language compiler and GAPP microcode generator. Starting at $37,000—including the PC AT—it will be available in January. ☐

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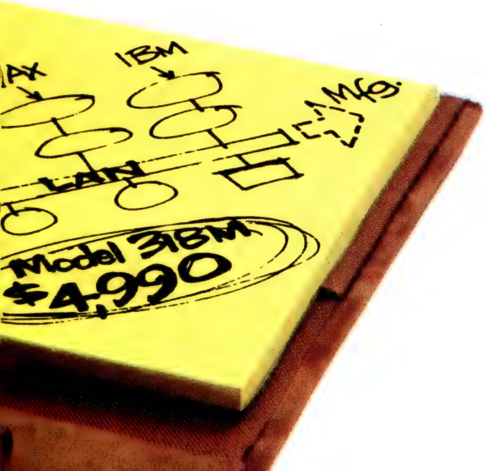

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Electronics

ASIC HOUSES RUSH TO ADD ANALOG FUNCTIONS TO LIBRARIES

MIXED CHIPS COULD TOTAL HALF OF 1990'S CELL-BASED MARKET

SANTA CLARA, CALIF.

It's turnabout time for the semicustom-chip market. After years of having digital integrated circuits chop away at the age-old turf of analog electronics, there is a sharply accelerating trend the other way as analog functions grow in many digital standard-cell libraries. Now, on-chip linear devices are becoming a key selling point in application-specific ICs.

The result is that demand for analog functions in ASIC libraries should continue to surge, says National Semiconductor Corp. National estimates that only $50 million of 1987's batch of cell-based semicustom chips will have some analog functions on board (see graph). But by 1990, nearly half of a cell-based ASIC market estimated to reach $3.5 billion will require analog functions, says Thomas Wong, strategic marketing manager for National's ASIC Division. Some projections are even higher. In Dallas, ASIC managers at National's archrival, Texas Instruments Inc., place the figure closer to 60%.

At least one TI executive admits to being amazed at his company's spiraling growth projections. "That number nearly floored me," says Tom Engibous, vice president in charge of TI's linear chip operation, which is handling the development of the LinASIC library.

No matter which estimate is more accurate, it's a sure bet that any market that could grow by some $2 billion in the next three years will get crowded in a hurry. And National has just become the latest to join the ranks of ASIC suppliers who are jumping on the bandwagon—among them some of the biggest names in the business.

The Santa Clara, Calif., chip manufacturer is rolling out the first linear building blocks for its standard digital 2-μm double-level-metal CMOS library. A leading supplier of analog chips, National is adapting basic linear functions for its standard digital CMOS process technology. The company is working too on additional technology modules—such as biCMOS and capacitor-oriented process steps—for high-performance analog functions.

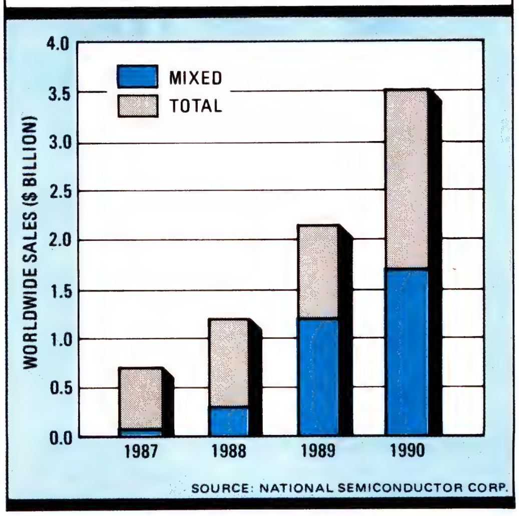
National joins an emerging movement among digital ASIC producers and linear-digital niche suppliers, who are scrambling to offer semicustom products spanning the spectrum of solid-state capabilities. TI, for example, is building a combined analog-digital cell library using a linear-oriented 3-μm CMOS technology. TI's LinASIC library now has 34 functions, and a bipolar module—called LinBiCMOS—is in the works for additional 20-V capabilities [*Electronics*, Sept. 17, 1987, p. 17].

Initially, TI is concentrating on using the library internally to speed up complex linear and custom designs. Several customers have begun using the LinASIC system for chips made in the linear-based CMOS process, which treats digital functions as a subset.

ANOTHER WAY. National is taking a different tack. It is enhancing standard analog functions for fabrication in 5-V digital CMOS technology. In the initial offering, National will include a number of products: three operational amplifiers with a bandwidth of 1 MHz, two comparators with response times of 150 ns, a 2.5-V voltage reference, an analog switch with 100 Ω of on-resistance, and a set of resistors for setting gain and voltage drivers.

More analog functions will be added around March, including a few medium-complexity macrocells. In the first half of 1988, "we will begin to look at adding more complex telecom functions, expanding the general range of analog capabilities," says Mike Bereziuk, director of marketing for the ASIC Division. Bereziuk believes the growth of analog functions in digitally dominated design libraries represents a critical factor in shifting total semicustom-chip sales toward cell-based ASIC by the early 1990s.

MORE ANALOG FUNCTIONS PUSH INTO CMOS ICs



SOURCE: NATIONAL SEMICONDUCTOR CORP.

Meanwhile, the movement to mix analog and digital macrocells comes as no surprise to those who were early in the field. NCR Corp.'s Microelectronics Division started offering simple analog macros in its CMOS cell library five years ago. The decision was fueled by requests from consumer-electronics houses wanting to cut pennies from their designs, recalls Gene Patterson, director of the semicustom business unit in Fort Collins, Colo. "Most of our mixed designs are mostly digital, with maybe 5% to 10% analog," he says. He estimates that as much as 30% of the ASIC chips sold by NCR have on-board linear functions.

At Sierra Semiconductor Corp. in San Jose, Calif., which entered the business expressly to mix analog with digital, the trend gets a mixed reaction. While it lends credibility to Sierra's decision to stake out the territory, it also means that competition is going to pick up. "I'm sorry to hear the big guys are finally catching on," says Mike Friedman, marketing manager. He thinks the key battleground for those who are mixing analog and digital on semicustom chips is the design-automation business, where Sierra offers a mixed simulator called MIXsim.

Sierra now has approximately 40 macro functions in its 2-μm CMOS library. As is the case with NCR, many of the additions to the library are coming as a result of requests from customers. Sierra plans to boost its chip integration and performance with a process shrink to 1.5 μm in 1988 and to 1 μm in 1989, he adds. *–J. Robert Lineback*

TELECOMMUNICATIONS

ISDN GENERATES NOISE AND SOME SIGNAL AT GENEVA

GENEVA

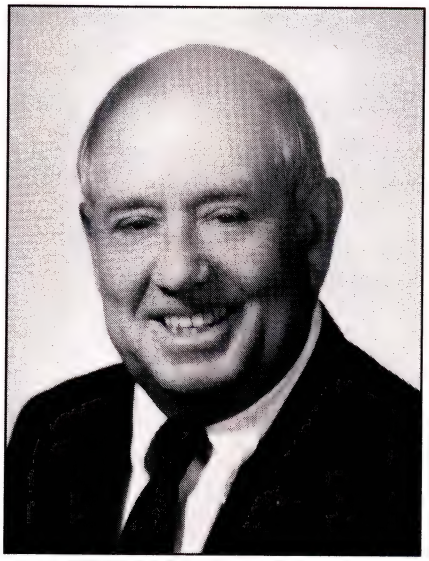
If what went on at Telecom 87 in Geneva was any indicator, the long-awaited Integrated Services Digital Network may finally be building to a critical mass. ISDN hardware bristled on the stands of telecommunications-equipment makers in Geneva in late October at the International Telecommunication Union's quadrennial "world's fair." The standards that could make ISDN a true global network still have to be hammered out, but based on the Geneva show the major players in the telecommunications business are learning how to work together.

At the Fifth World Telecommunicatons Exhibition, 30 of the world's top computer companies, telecommunications switch suppliers, and service providers joined forces in an imposing stand that showed the heady potential of ISDN—combinations of speech, text, data, and image carried on the telecommunications line.

Significantly, the joint-venture stand was not a razzle-dazzle demonstration with everybody's gear linked to everyone else's. Chalk that up to the lack of common standards. "We nod in agreement that ISDN is the key to building a global information age network. But when all is said and done, the fact remains that common implementation standards for ISDN do not exist," AT&T Co. board chairman James E. Olson told the Executive Telecommunication Policy Symposium at Telecom 87. "Our customers won't tolerate it," Olson added. "They are not asking what our technology can do for them in theory. They're asking what it can do for them in the workplace to solve real problems."

While awaiting standards, some major players are pushing to turn their gear into de facto standards. And even without standards—official or otherwise—heterogeneous groups of vendors and telephone companies are putting together working ISDN networks built around a central switch linked to a variety of terminals and private branch exchanges.

Digital Equipment Corp., for one, has a de facto standard in mind. At Telecom 87, the Maynard, Mass., computer maker announced its Computer Integrated Telephony program. Under this scheme, an ISDN link is established between a PBX and a VAX computer attached to an Ethernet-type local network.



PRESSED. AT&T board chairman James Olson says customers want ISDN in a hurry.

This allows applications programs to be written for the VAX combining voice and text or data services, such as identifying unanswered calls. "The concept of doing it independent of PBXs is new," says Alex Zwahlen, DEC's field programs manager for networks in Europe. "Previously, if you were doing a scheme like this, you'd most likely have to throw out your PBX and phones."

DEC has already agreed on an ISDN interface with PBXs from Northern Telecom and British Telecom. It also has similar deals in the pipeline with Siemens, Philips, Ericsson, and Plessey. It plans a common user interface in the VAX so that independent software houses can develop applications for any PBX.

Siemens AG, too, made a move for de facto status at Geneva. Its PBXs are often used for experimental interfaces and the West German firm is trying to establish its signaling system for private networks, dubbed CorNet, as the basis for an international standard. But it is likely to run into opposition from the British, who are already implementing their own standard, called Digital Private Network Signalling System.

In any event, lack of standards has not held back equipment makers who want to prove their gear can be linked to hardware from other manufacturers.

Canada's Northern Telecom Ltd., for example, showed at Geneva how its switches can interface at the 144-Kbit/s basic rate with gear built by IBM, Fujistsu, Apple, Hayes, Harris, Hewlett-Packard, DEC, and Motorola.

At the Japanese pavilion, Nippon Telegraph & Telephone Corp. linked a D700 switch from Fujitsu Ltd. with 13 terminals and PBXs from 13 Japanese manufacturers to carry services ranging from a picture phone to high-speed facsimile and high-resolution videotex. Three of the manufacturers, Fujitsu, Hitachi, and NEC, demonstrated the compatibility of their 2-Mbit/s primary-rate ISDN interfaces to switches in their booths.

Not to be outdone, the Swiss PTT, which had put a Siemens EWSD digital switch into service in Geneva shortly before the show, used it to demonstrate services combining text, data, speech, and images on terminals from Canon, Alcatel, and Telenorma.

On the eve of Telecom 87, IBM and Nynex announced similar joint trials in the U. S., the first in which IBM has participated. An ISDN link will be installed between one of Nynex's central switches and its New York research and development laboratory, using experimental ISDN interfaces in IBM work stations.
–Peter Heywood, McGraw-Hill World News

THE MARKET

AFTER THE CRASH: THE SMALL FIRMS ARE HURTING

NEW YORK

The U. S. electronics industry is still assessing the fallout from the Oct. 19 stock-market meltdown, but one thing is certain: the hardest hit were the small, emerging companies that look to the stock market for fresh capital.

These companies—especially those planning stock offerings for this fall and winter—are now effectively locked out of the market for at least six months. "Companies, and we are not just talking about startups, depend upon the stock market year after year after year for capitalization," says Charles V. Prothro, the Dallas-based venture capitalist who founded Dallas Semiconductor. A sudden, rapid market decline "means that source is closed off for the small companies. It is exceedingly dangerous and a terrible signal to those young companies, which have no way of getting the cash once they've gone past the resources of venture capitalists."

Dozens of small- to medium-sized businesses were affected. Altera Corp., the Santa Clara, Calif., programmable-logic firm, had planned a public offering for late October. Orchid Technology of Fremont, Calif., a maker of local-area networks and graphics boards for personal computers, was seeking to raise $17 million with a late fall stock issue. Also caught in the squeeze were Metaphor Computer Systems Inc., a Mountain View, Calif., maker of information-retrieval systems; Relational Technology Inc. of Alameda, Calif., which sells database-management software, and many others. They all face what could be a delay of six months or longer in their attempts to issue stock, says Bruce Entin, a vice president at LSI Logic Inc. of Milpitas, Calif.

"The ability of companies to go to the market for money will be severely limited," Entin says. "That is going to have major implications for privately held companies that were in the midst of filing plans" to issue stock.

Some did manage to get in under the wire, however. Dallas Semiconductor Corp. was perhaps the last chip company to go public before the crash, raising $36 million in much-needed funds on Oct. 6. But as the company's shares slipped from a high of $11.25 to less than $6, worries began to surface. "It's hard to build a company for nearly four years, and then suddenly, in hours, have its value plunge," says Michael Bolan, vice president of marketing.

Some market observers are optimistic that the damage is only temporary. And larger firms, like Xerox and Prime Computer, were able to make some hay out of the situation by aggressively buying back their own stock. That helped prop up their market value while reducing the equity in public hands.

These bigger firms should not be badly damaged, says Adam Cuhney, a senior analyst covering semiconductors for Kidder, Peabody and Co. in San Francisco. "Business continues to be strong and I feel really good about prospects," he says, adding that semiconductor stock prices should recover much of their lost value quickly.

Stephen Coit, general partner of Merrill, Pickard, Anderson & Eyre, a Palo Alto, Calif., venture-capital firm, says jolts such as the Oct. 19 stock market plunge periodically take their toll. Says Coit from his Waltham, Mass., office, "There's a Darwinian process that hits every two to three years, weeding out some of the weaker players." But Coit offers a word of advice: "Companies that have focused on self-reliance—who aren't spending beyond their means—usually survive these things."

– Tobias Naegele with bureau reports.

SUPERCOMPUTERS

U.S. GETS STRONGER IN SUPERCOMPUTERS

ST. PAUL, MINN.

Make no mistake about it: the U. S. is still winning the supercomputer war. Latest evidence came last week when ETA Systems Inc. offered striking proof that it was no longer a paper tiger. Add to that two new U. S. competitors—CHoPP Computer Corp. and SuperComputer Systems Inc.—and the picture gets even rosier. Industry observers agree that these three U. S. companies coupled with industry leader Cray Research Inc. should have the technical muscle and the manufacturing capability to maintain the U. S. lead in supercomputers over their Japanese competitors, Fujitsu, Hitachi, and NEC.

ETA's coup last week was in introducing a pair of high-performance air-cooled machines so aggressively priced that they set price/performance records for supercomputers [*Electronics*, Oct. 15, 1987, p. 22]. The machines, plus two faster liquid-nitrogen-cooled models, create a family that now positions ETA, the St. Paul, Minn., subsidiary of Control Data Corp., as a major contender for supercomputer business worldwide.

The two new companies should also prove to be formidable foes. CHoPP, in LaJolla, Calif., plans to introduce its CHoPP 1 early in 1988. Targeted at the high end of the performance range, the machine will have 4 to 16 processor nodes and performance ranging up to 10 times that of the fastest current-generation machines, such as the Cray X/MP series, CHoPP claims.

The other startup, SuperComputer Systems, is newly established in Eau Claire, Wis., by Steven Chen, who recently quit Cray [*Electronics*, Sept. 17, 1987, p. 21]. The company's business plan is to bring a new high-end supercomputer to market, but no details are available. Chen left Cray when the advanced MP system he had been working on since 1985 was canceled; he plans to continue the work he began there.

Industry observers agree that all these U. S. companies have the technical muscle and low-cost automated manufacturing capability to keep the U. S. industry strong and in the lead ahead of the three Japanese contenders, Fujitsu, Hitachi, and NEC.

With ETA's new machines, "pricing is very aggressive and about what we expected, but the performance specifications were greater than expected," says Jeff Canin, analyst with Hambrecht & Quist, the San Francisco venture-capital company. The entry-level ETA10-P

TAKING AIM AT THE REAL-TIME MARKET

As new supercomputers from ETA Systems Inc., CHoPP Computer Corp., and SuperComputer Systems Inc., move from design into production and start fighting it out in the vector-supercomputing market dominated by Cray Research Inc., a Colorado Springs, Colo., startup called Prisma Inc. plans to launch an attack on a different front: real-time scalar supercomputing.

Prisma is building a gallium arsenide-based system that relies on a 32-bit reduced-instruction-set architecture. With it, the company hopes to grab the lead in what it believes is a growing niche for supercomputers that can handle real-time tasks in embeddable applications. In contrast, most supercomputers are vector machines best suited to do simulation; their speed is measured in millions of floating-point operations a second, or megaflops. Scalar models are slower, working in millions of instructions per second, or mips.

Using GaAs chips supplied by Gigabit Logic Inc. of Newbury Park, Calif., Prisma plans late 1989 shipments of multiprocessor systems that can hit 250-mips peak performance per processor, with sustained rates of 150 mips per processor. By contrast, a single-processor Cray X/MP, which is optimized for vector performance, can hit a peak of only about 33 mips, says Philip Gerskovich, Prisma cofounder and a former Cray Research engineer. The next nearest competitor, he says, is Elxsi, San Jose, Calif. Its 1-to-12 processor System 6400 performs at about 4 to 12 mips per processor [*Electronics*, April 2, 1987, p. 34].

While Elxsi and its competitors sell systems primarily for equipment such as military simulators, Prisma says it is aiming at embeddable applications such as phased-array radars, intelligent battle management, and systems to be used in the Defense Department's Strategic Defense Initiative. A typical single-processor Prisma system with about 16 megabytes of memory will occupy less than a cubic foot of space and dissipate 1 to 5 kW, Prisma says.

Gerskovich says prices for the Prisma machines are expected to range from about $500,000 for a single processor with a minimum 128 Kbytes of memory, up to about $5 million for a four-processor machine that comes with up to 64 Mbytes.

–Wesley R. Iversen

model delivers full supercomputer performance of 375 million floating-point operations per second and 25 megaflops on a Linpack benchmark for under $1 million. "It is clearly the highest performance at that price," says Canin.

A complete ETA10-P system, including a disk drive and software, is available at a special package price of $995,000, putting it within the means of some departmental-level purchasers. Its performance, however, is at the level of full supercomputers costing between $5 million and $20 million.

For example, when running a standard linear equation benchmark, the Linpack 100-by-100 64-bit Fortran case, the ETA10-P is several times faster than several minisupercomputers that are competing in the same price range. It is eight times faster than a Convex C-1/XP and about three times faster than an Alliant FX/8. The second new machine, the ETA10-Q, is also air-cooled and runs at a faster clock speed than the model P: 19 ns, compared with 24 ns for the model P.

Both use the same central processor board as the two big nitrogen-cooled ETA10 systems, the model E introduced earlier and the model G coming next year. The ETA10-E is the fastest computer in the world, its 10.5-ns speed running the Linpack 100-by-100 matrix at 56 megaflops. When the 7-ns ETA10-G becomes available, it is expected to run the same benchmark at 84 megaflops. The two machines closest in speed are the NEC SX-2, running at a speed of 43 megaflops, and the Cray X-MP/4, running at 39 megaflops.

One advantage of the newly expanded ETA10 product line is compatibility from the model P up to an eight-processor ETA10-G8, a 10-gigaflop machine at $22 million—a performance range of 27 to 1. "The one handicap is the lack of third-party applications software," says Canin. "More applications will have to be made available before a strong demand will materialize." *–Tom Manuel*

CHIP PROCESSING

NEC DRAWS 0.2-MICRON LINES WITH X-RAYS

TOKYO

West German scientists who believe they're a year or two ahead of the rest of the world in X-ray lithography had better look over their shoulders at Japan. Tokyo-based NEC Corp. now says it has put together a system that can achieve 0.2-μm line widths. The best test devices reported out of Germany have 0.35-μm geometries [*Electronics*, Feb. 5, 1987, p. 78]. What's more, NEC reports impressive throughput: it can apply patterns to 25-by-25-mm areas on forty 8-in. wafers per hour.

Because of its throughput, the NEC system (see figure) bodes to become a workhorse in about three years when the synchrotron rings it uses for an X-ray source become generally available. The parallel synchrotron radiation source with 100 times the strength of conventional X-ray systems is a key to the system's performance, says Kazuo Ayaki, vice president of NEC's Research and Development Group. Parallel radiation—the rays neither diverge nor converge—makes it possible to easily use conventional optical steppers—they are available in LSI production facilities, and optical masks are easier and cheaper to make than X-ray masks—for the lower-resolution layers, while its high output shortens exposure time.

SOLVING PROBLEMS. The system hurdles the major obstacles to high-volume X-ray production. First, it performs its lithography with the masks and wafers in air, eliminating vacuum locks. Second, since each device on a wafer is smaller than the 25-by-25-mm field covered by the X-ray beam, the system can lithograph many patterns on the wafer simultaneously. This means fewer steps and alignment problems, and better yield and throughput.

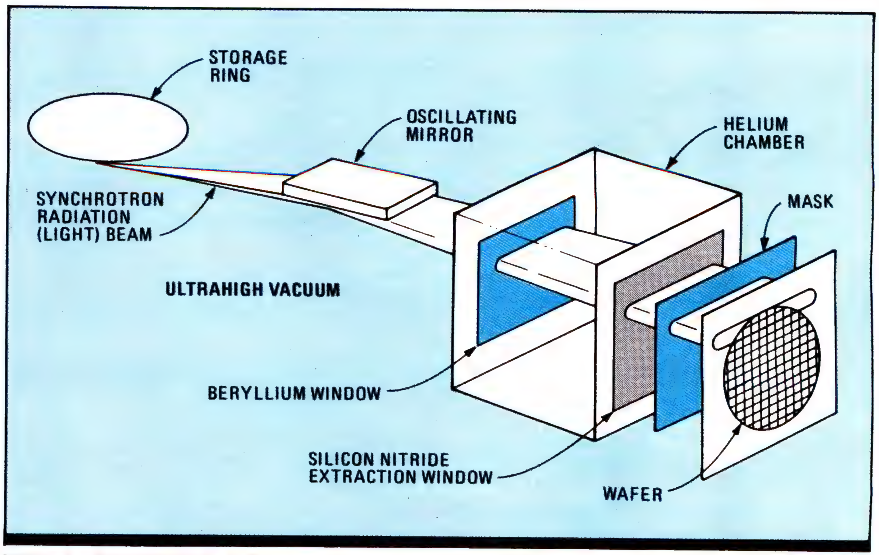
Keeping the masks and wafers in air is a major advance, particularly since the designers had to deal with the fact that air attenuates X-ray beams. The upshot is that many experimental systems insert the masks and wafers into a vacuum chamber, which requires a system of airlocks. This increases the number of operations required to load and unload, slowing the procedure.

TRANSITION CHAMBER. So the NEC engineers did two things. First, they provided a transition chamber between the high-vacuum system and the mask-and-wafer arrangement for the beam to pass through. The chamber is filled with helium at atmospheric pressure, which does not significantly attenuate the X-rays. Second, they minimized the distance that the beam has to travel through air by placing the wafer to be exposed just 10 mm from the chamber's extraction window.

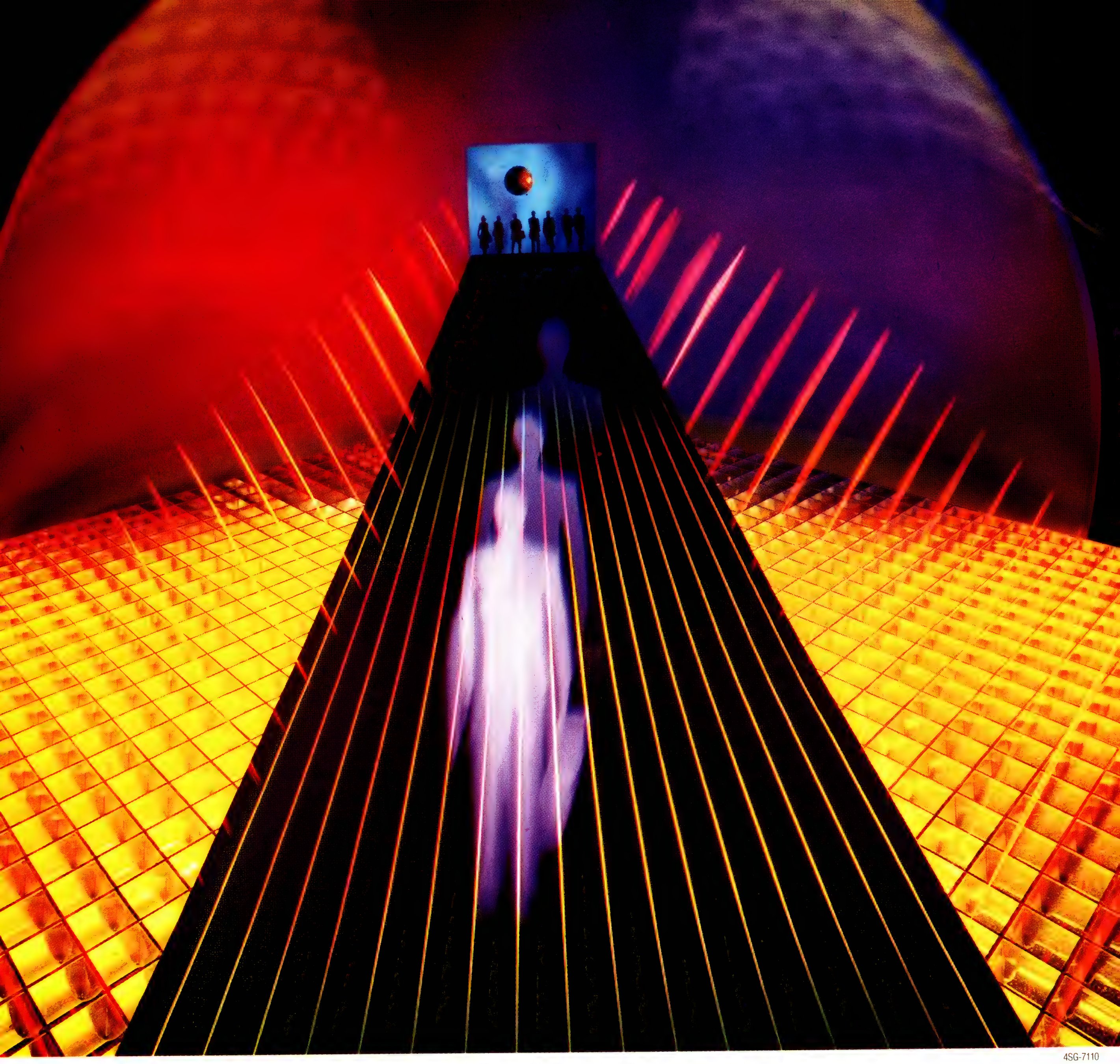
The window between the high-vacuum system and the helium-filled transition is a 50-μm-thick sheet of beryllium, which is highly transparent to X-rays. Although this window must withstand the pressure of one atmosphere of helium, it's not degraded as it would be if one side were in air. Also, circulating helium cools the beryllium, preventing heating caused by the slight X-ray attenuation.

At the other, or extraction, end of the transition chamber is a window of 3-μm-thick silicon nitride, which has reasonably low attenuation and does not decompose in air. This window can be extremely thin because of the balanced pressure on both sides. X-ray attenuation is minimal. Silicon nitride, with patterned tungsten as the absorber, is the material used for masks for lithography.

Work on the lithography system is independent of the development of the synchrotron ring itself. NEC is a member of Sortec [*Electronics*, Aug. 7, 1986, p. 44], whose 13 members are jointly developing rings. *–Charles L. Cohen*



WITH A LIGHT TOUCH. NEC's high-throughput X-ray lithography system uses a synchrotron ring as its light source, giving it 100 times the strength of conventional X-ray systems.



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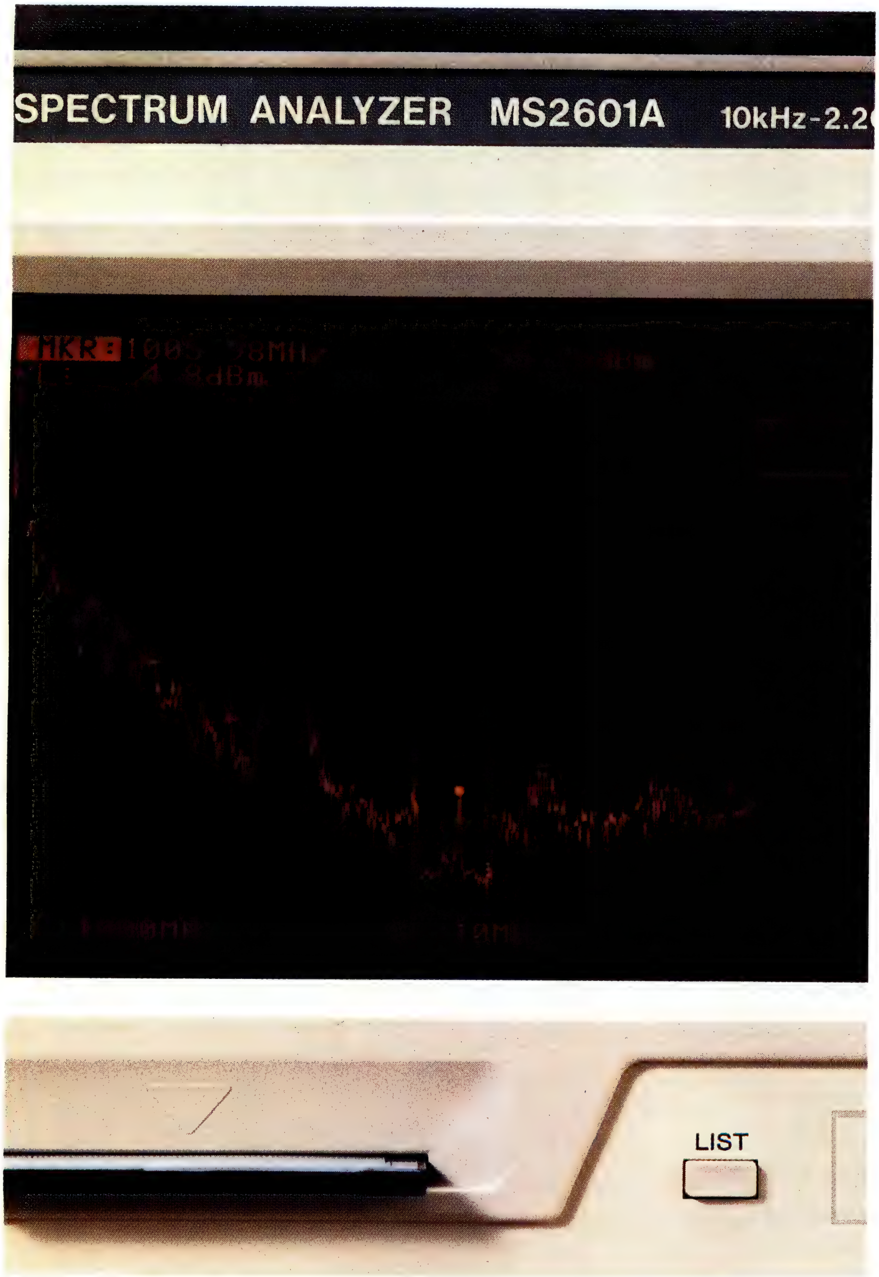

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IC TESTING

IBM TESTS SILICON CHIPS BY PHOTOEMISSIVE SAMPLING

ZURICH, SWITZERLAND

Contactless testing of high-speed chips with laser beams is an international game of one-upmanship. And now the experts at the IBM Corp. Research Laboratory in Zurich have gone their competitors one better: their new photoemissive sampling technique measures signals not only on gallium arsenide but on silicon chips as well.

Most of the work going on in the field—at AT&T Co.'s Bell Laboratories, Aerospace Corp., Stanford University, and elsewhere [*Electronics,* June 11, 1987, p. 36]—is aimed at GaAs chips. "But the semiconductor world is still one of silicon and will be for some time to come," says Hansjörg Beha, co-inventor of the IBM approach and head of the Zurich team. "So a method for broader applications, and unrestricted to a specific substrate material, is in demand."

Prompting the efforts to develop noninvasive IC test schemes are the limits posed by mechanical probes. As circuit dimensions shrink, it gets more and more difficult to point probes at a circuit's internal nodes—the limit of accuracy is about 1 μm. It is also difficult to place the probe under a microscope, and there is a risk of the probe's damaging the chip.

So Beha and his three-member group began implementing what they call the ICLT (for integrated-circuit laser-testing) method two years ago, and the results are impressive. With a laser beam 1 to 2 μm in diameter, the technique measures signals as short as 5 ps. The voltage resolution—that is, the smallest measurable potential difference—checks in at 10 mV, and it takes 10 to 40 ms to measure such ultrafast signals. The fastest rise time the IBM researchers have measured is 11 ps.

IBM's photoemissive technique measures signals down to 5 ps

By comparison, commercial electron-beam systems, the other contactless way to test both silicon and GaAs chips, can measure signals around 100 ps, and take up to 1 s to determine a 10 mV pulse at a point on the chip. On top of that, there is the chance of errors from the electrical charges that the e-beam produces in the IC's insulating material.

The IBM team is scaling down the beam diameter for lines smaller than 1 μm. It is also aiming at a better time and voltage resolution. Still another goal is a test setup that does away with the vacuum chamber, cutting equipment costs and simplifying measurements. Beha will reveal the results of this new work at the First European Conference on Electron and Optical Beam Testing of Integrated Circuits in Grenoble, France, Dec. 9 to 11.

In contrast to the GaAs chip-testing method, which exploits the material's electro-optical behavior, the new IBM technique is based on photoemission. This phenomenon, discovered by Einstein, allows testing to be independent of circuit technology or substrate material. Light, or photons, impinging on a material induces the emission of electrons if the photon energy exceeds the work function of the illuminated material. For the metallic materials used as conductors in ICs—aluminium, aluminium-copper alloys, or polysilicon—the work function is typically 4 eV. Emission occurs when the photon energy is in the ultraviolet range at which it exceeds the 4 eV.

Attracting the electrons emitted from the illuminated spot is a wire grid that is installed about 1 mm above the chip and held at a positive voltage. If this grid is at a constant potential, the changes in the electrons' acceleration to the grid is a measure of the voltage changes at the point of emission. Signals and logic states can be determined at that point.

The IBM setup uses a mode-locked argon-ion laser that pumps a dye laser to produce 1-to-2-ps pulses with a photon energy of 2.5 eV at a 4-MHz repetition rate. Then the frequency is doubled to bring the wavelength down into the ultraviolet range at 250 nm and the photon energy up to 5 eV. This energy, now exceeding the material's work function of 4 eV, is enough to induce electron emission. *–John Gosch*

RELATIONAL DATA BASES

A COPROCESSOR THAT'S A DATA BASE

SANTA MONICA, CALIF.

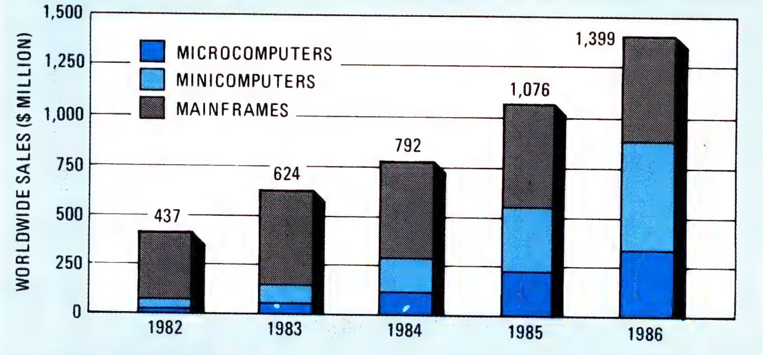
Relational data bases, which store data that indicate the relationship between items in separate data files, have become a big software business. Now a startup company named Nucleus International Corp. has come up with a way to do the job in hardware instead.

Nucleus's innovation is N:vector, a relational data-base engine in the form of a plug-in board for IBM Corp. PC ATs and compatibles that employs five custom gate-array chips with a streamlined data-base scheme. The Santa Monica, Calif., company says its board—actually a coprocessor—can do a job 10 times faster than the purely software solutions. What's more, say Nucleus executives, N:vector has a proprietary associative storage system that takes up only one tenth the space of any of its software counterparts.

Relational data bases represent about 60% of the total data-base market, and Nucleus is aiming at what it estimates to be the fastest-growing part of the business (see figure). The company says sales of data bases for microcomputers climbed to $315.2 million in 1986, up from $219.3 in 1985. Nucleus is also planning versions of N:vector for minicomputers, whose data-base sales grew to $554.1 million in 1986 from $316.9 the previous year, and for mainframes, which saw sales slide to $529.9 in 1986 from $539.9 in 1985.

The Nucleus technol-

MINIS AND MICROS GAIN IN THE DATA-BASE MARKET



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ogy, first shown to original-equipment manufacturers in mid-October, should make waves in the marketplace, predicts E. F. Codd, founder of the Relational Institute, a data-base consultant in San Jose, Calif. "Building into hardware [the] operations you expect in a fair amount of software is a drastic new way of doing things," at least for personal computers, he notes.

N:vector is the brainchild of Edward L. (Ted) Glazer, Nucleus's co-chairman and chief technologist, who holds more than 30 computer-related patents, most notably one for the light pen. It is based on bit vectoring, a mathematically concise way of representing sets of data as vectors, or streams, of binary information. With bit vectoring, N:vector data values need be stored only once, compared with several times in conventional data bases. And when a value is changed, which is a common data-base operation, the change is reflected simultaneously in all references, saving both time and storage space.

Data values need only be stored once with this new approach

"This structure provides enormous efficiencies in both processing speed and memory requirements," observes Glazer. For example, because the Nucleus board uses data-compression techniques, its 512 Kbytes of random-access cache memory actually equal up to 5 Mbytes of RAM in conventional data-base systems, he says. In practical terms, most minicomputer data bases run into trouble handling upward of 30,000 entries (or complex queries). But the N:vector technology can accommodate more than five times that number, says Glazer.

But Nucleus's path to the bank isn't obstacle-free. There are many software data-base products in end-user distribution channels, and high-priced front-end computer hardware is already on the market. Nonetheless, Nucleus believes its offering is "complementary to the OEM computer world," says Derek W. McLeish, vice president of marketing. He adds that N:vector has the standard SQL (structured query language) interface. He predicts that even seemingly competitive vendors of relational database software could use the engine to enhance their wares.

One of them, Ashton-Tate Corp. of Los Angeles, has its doubts. Though N:vector is a good retrieval system that can fill a definite niche, it has no multiuser capability, says Willem Stoeller, director of advanced development, who worked at Nucleus more than a year ago. Nevertheless, Nucleus says it has

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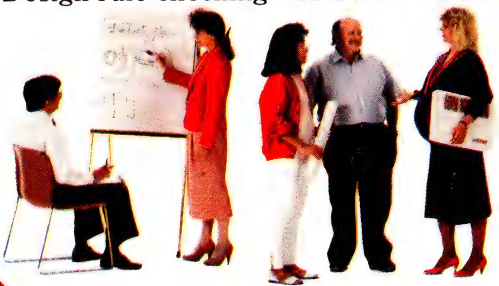

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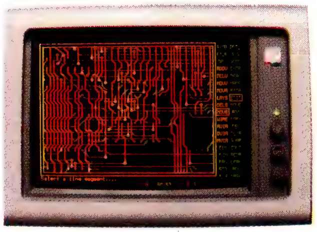

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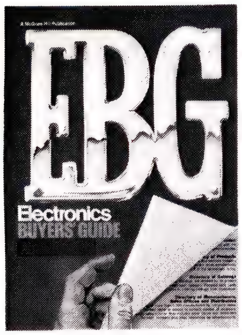

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already lined up several OEMs and has its first boards in beta sites. Nucleus will supply an entire development system for about $10,000. McLeish says the cost of end products might be about $3,200 per user. By contrast, Ashton-Tate's dBase sells for about $700 and the SQL-based data-base management system from Oracle Corp. of Belmont, Calif., is priced at nearly $1,300.

–Larry Waller

SOFTWARE

WHY AT&T AND SUN HOOKED UP

NEW YORK

Like a sheriff rounding up a posse, AT&T Co. is corralling some key Unix players to chase after a bigger share of the midrange computer market. In its second major announcement in six weeks, AT&T's struggling Data Systems Group said last week that it is joining forces with Sun Microsystems Inc. of Mountain View, Calif., to develop a unified version of its Unix System V and SunOS, Sun's derivative of Berkeley Unix 4.2 bsd. In September, AT&T announced a similar deal with Microsoft Corp., under which the two companies are merging all the features of Microsoft's Xenix operating system into AT&T's System V.

These moves seek to establish System V as the de facto Unix standard in a confusing marketplace abounding with different and incompatible versions of the operating system originated at AT&T. At the same time, AT&T hopes some of the marketing strength of users such as Sun will add muscle to its computer line. However, whether AT&T can get other key players to join in consolidating the Unix world will be the true test of that strategy.

But that is not much of a strategy, figures analyst Jocelyn Young of Future Computing Corp., a Dallas market researcher. "They realize they can't go it alone," she says of AT&T, "so they're trying to leverage some of the market presence of the other players in the Unix and Xenix market," and to establish Unix V as the standard.

BOTH GAIN. Drawing others in may not be easy, but in joining up, AT&T and Sun are hoping that together they can do what neither could do alone. While the deal gives AT&T a bigger role in consolidating the Unix environment, it offers Sun a key backer in its effort to make its Sparc (Scalable Processor Architecture) microprocessor an industry standard for reduced-instruction-set computing. AT&T Data Systems Group president Vittorio Cassoni says AT&T

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will eventually use the Sparc architecture across its entire line of minicomputers, but the first system to use the chip is still at least two years off.

AT&T's push to expand System V to include features of other Unix versions comes along just as the Institute of Electrical and Electronics Engineers and X/Open—a consortium of European computer companies—are getting closer to defining their own standards. AT&T is not trying to upstage those efforts, says Michael DeFazio, director of software systems for the Data Systems Group. He says, however, that neither standardization effort goes far enough, and he promises that AT&T will incorporate within its expanded System V interface definition, called SVID, any features required by either new standard. That should be simple, DeFazio says.

Sun gets a key backer in the drive to standardize its RISC chip

The IEEE Posix standard, which is now in draft form, "deals with one volume, one third of the SVID standard," he says. "About 75% or 80% of that is precisely SVID, and the rest is Berkeley extensions." The X/Open standard, which is still in the definition stages, will also be based on SVID.

The enhanced System V, which will be developed by AT&T, will be optimized for the Sparc computing platform, incorporating features from System V, Berkeley 4.2, and SunOS. Sun's Network File System, its variation of the X-Windows graphics interface, NeWS, will also be included.

AT&T has struggled as a computer maker since it was allowed to enter the business after the breakup of the Bell System in 1984. The company had some early success with its high-end IBM-compatible personal computers, but more recently has lost money with both those products and its 3B line of mid-range machines. At the same time, it has drawn heavy criticism from analysts who complain that AT&T lacks a coherent strategy for computers.

These analysts give mixed reviews to the latest moves by AT&T, and not all of them are convinced that these moves are evidence of what group president Cassoni calls "a concerted effort to consolidate the Unix-system market." For example, Kenneth Bosomworth, president of International Resource Development Inc. of Norwalk, Conn., says that AT&T is merely "ringing doorbells." In his view, "Sun's answer indicates that they opened their door. It takes them [AT&T] nowhere; it's a mindless strategic alliance." *–Tobias Naegele*

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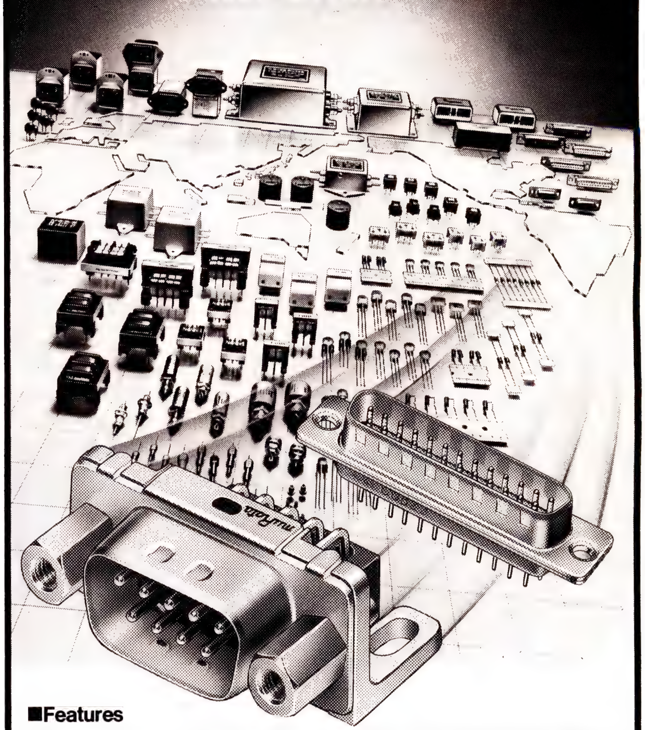

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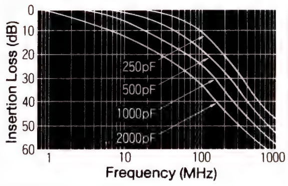

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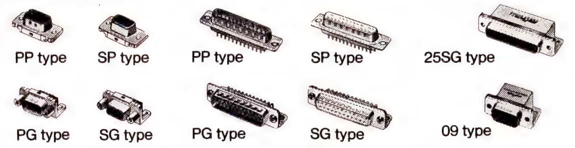

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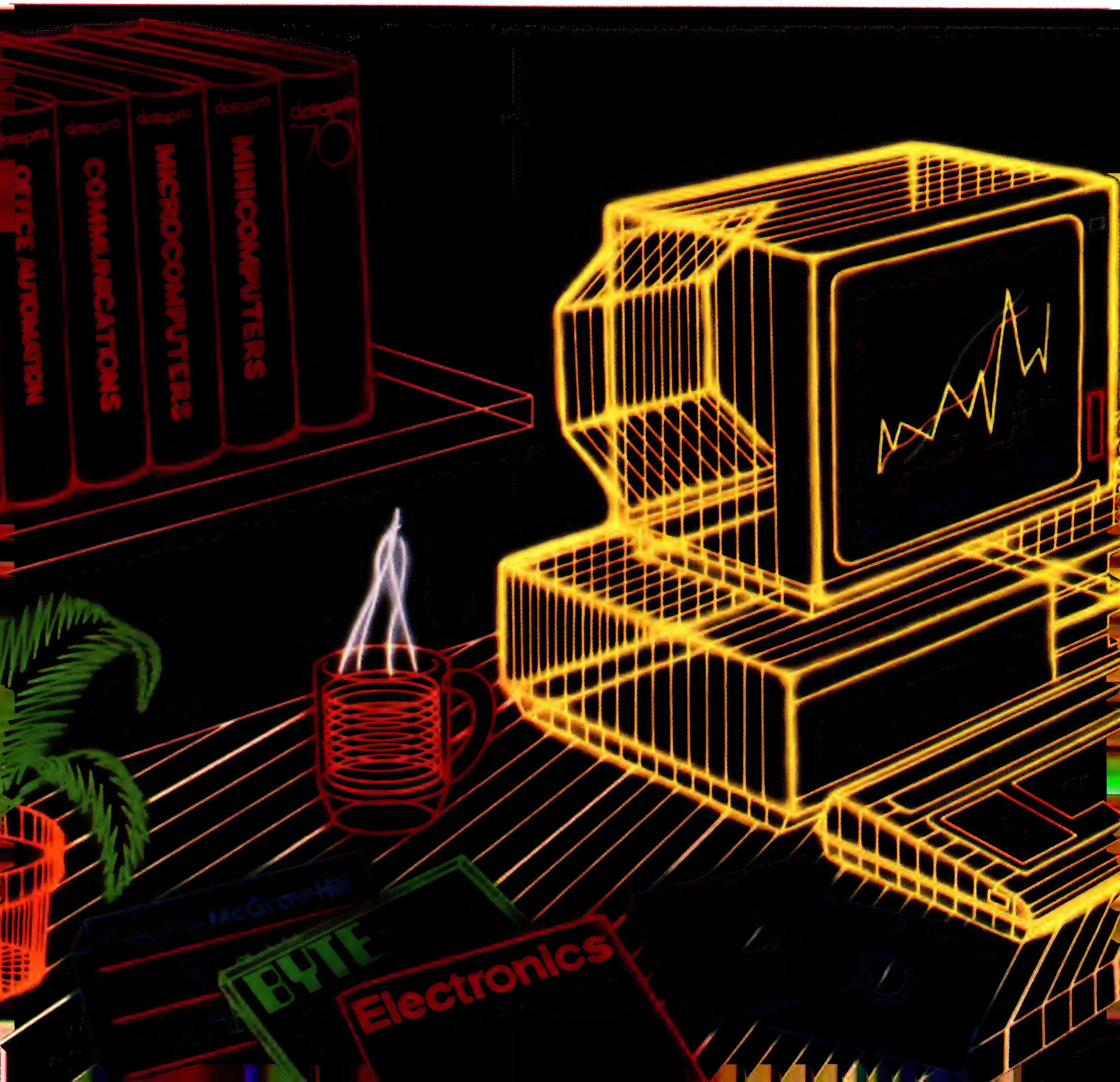

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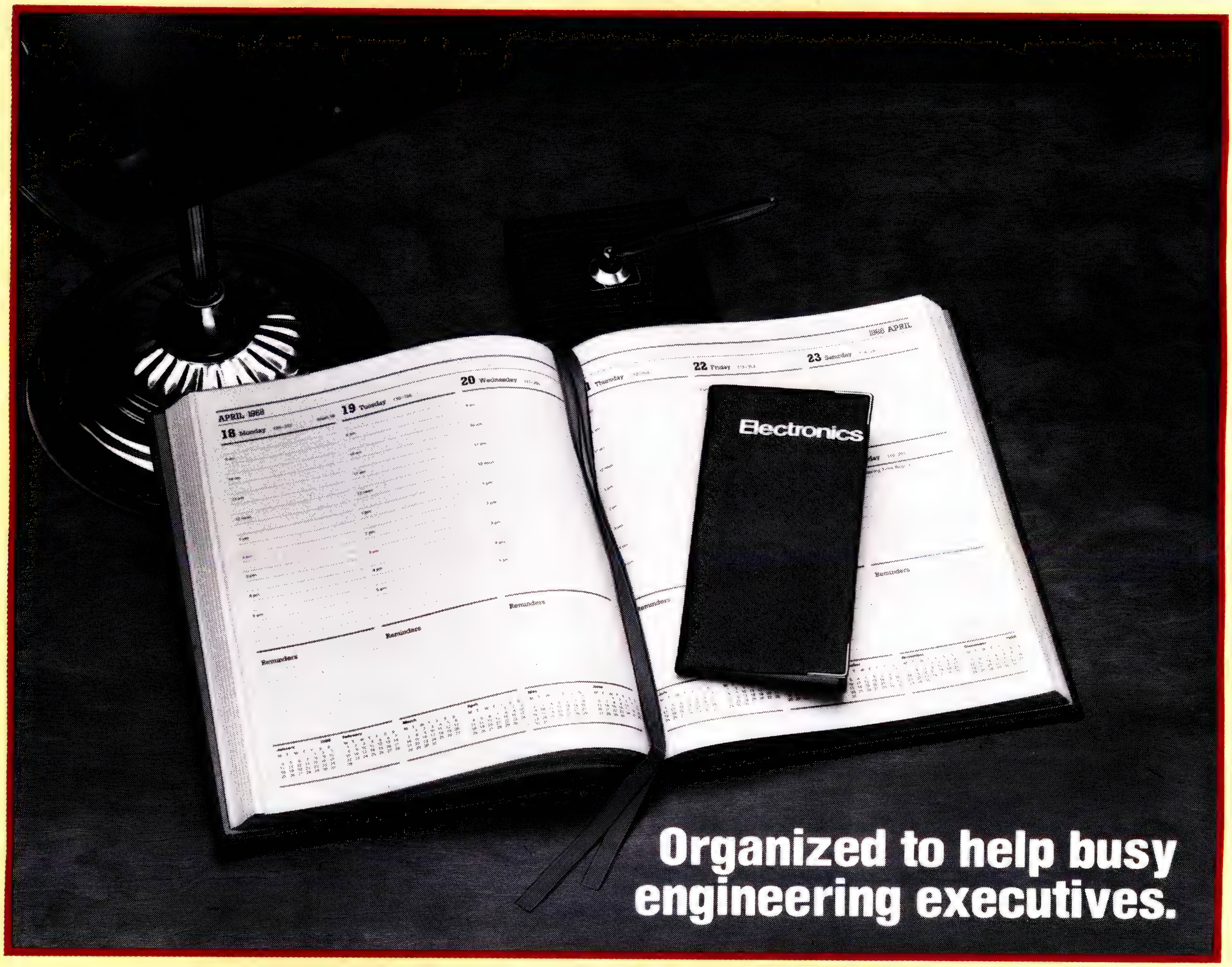

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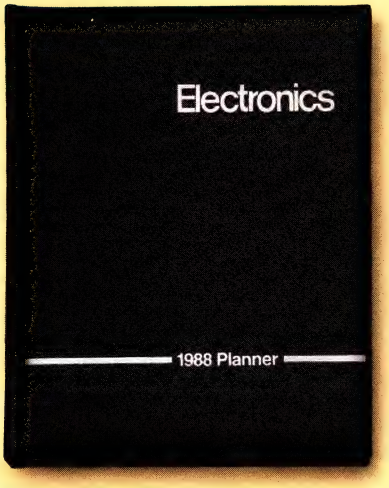

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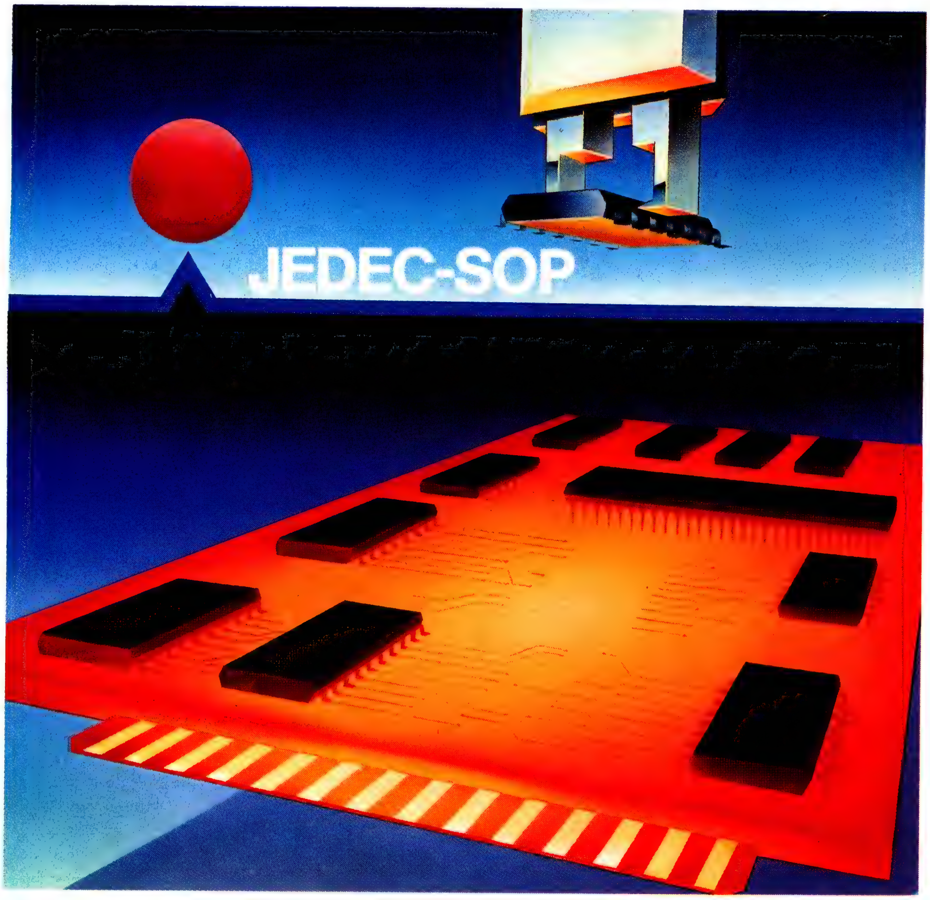

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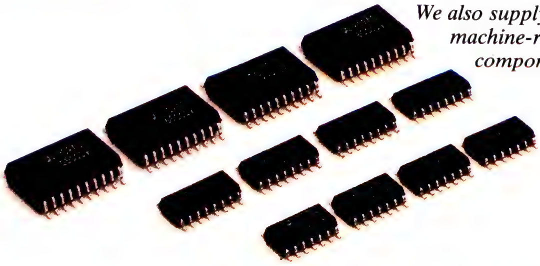

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OCTOBER 29, 1987

INTERNATIONAL NEWSLETTER

EAST GERMANS GET A 256-KBIT DRAM INTO PRODUCTION

Western nations have embargoed shipments of 256-Kbit dynamic random-access memories to Eastern Bloc countries, but now there's a source behind the Iron Curtain. VEB Carl Zeiss Jena in East Germany is producing 256-Kbit, 1.5-μm CMOS DRAMs. The chips put East Germany on a par with, or even ahead of, most Western European countries. Western observers rate the level of sophistication of East Germany's electronics industry as among the highest in the Eastern Bloc, trailing perhaps only that of the Soviet Union. Much of the credit in the memory field goes to the know-how Carl Zeiss Jena has gained in optical equipment in its 141-year history. The combine has been successful in transferring this expertise to chip lithography. It is now eyeing the production of 1- and 4-Mbit DRAMs. □

FUJI ELECTRIC CRAMS AUTOFOCUS SYSTEM ON ONE CHIP

January should see the beginning of mass production of a sophisticated autofocus chip by Fuji Electric Co. The chip will integrate a focusing sensor, an analog-to-digital converter, memory, logic, processing circuits, and output circuits, and should allow the manufacture of smaller, lighter, and cheaper autofocus cameras of the type with between-the-lens shutters, says the Tokyo company. Most autofocus cameras are built with parts from Honeywell Inc., Minneapolis, Minn., but Honeywell will also profit from cameras made with Fuji Electric's circuit. The chip is based on Honeywell's patented autofocus technology, and the Japanese company will be paying Honeywell royalties under a license signed in September 1986. Honeywell, meanwhile, is engaged in a patent-infringement dispute with another Japanese camera maker—Minolta Camera Co. of Osaka—over the through-the-lens autofocus technology used in its cameras. □

CASIO SLASHES THE COST OF ELECTRONIC STILL CAMERAS...

Casio Computer Co., Tokyo, is about to dramatically reduce the cost of cameras that record still images electronically. It will offer a complete color electronic still camera, the VS-101, for around $900, some 60% below the price of professional still video cameras on the market from such companies as Canon Inc. and Fuji Photo Film Inc. Industry observers, however, expect the Casio camera's picture quality to be somewhat lower. The 960-gram Casio camera has a 280,000-pixel image sensor and a 2-in. floppy-disk drive and is the first such product that can be connected directly to a television set for image viewing. □

...AND MINOLTA ADDS AN ELECTRONIC-STILL OPTION FOR SLR CAMERAS

Taking another tack, Minolta Camera Co., Osaka, will soon offer a special back for its line of autofocus single-lens-reflex 35-mm cameras. This add-on option lets a standard camera record images electronically with a 380,000-pixel charge-coupled-device color image sensor and a 2-in. disk drive. Also in the back is a relay-lens system that reduces the image size for capture by the sensor, which is much smaller than a frame of 35-mm film. Images captured by the $1,400 camera back can be reproduced by a color video printer ($1,200) or shown on a television set via another unit, called a still video recorder (also about $1,200). With the new product, Minolta will join two other camera makers in the new trend toward electronic still cameras that record an entire video frame, which is comprised of 480 effective scan lines, instead of a video field—half of an interlaced video frame, and thus only 240 effective lines. Sony Corp. introduced a camera with this capability in August for about $3,400, and Konica Corp. followed with a $2,800 unit in September. □

INTERNATIONAL NEWSLETTER

UK PLANT GEARS UP ADVANCED PROCESS TO PRODUCE OPTICAL DEVICES

Within a few weeks, newly designed equipment for an advanced metallo-organic vapor-phase epitaxy process will ramp up to full commercial production of optoelectronic devices based on indium phosphide in Ipswich, UK. BT&D Technologies, a joint venture of British Telecom Research Ltd. and Du Pont's Electronics Division, Wilmington, Del., has developed its own epitaxy equipment, which it says achieves high reproducibility and tight control over the thickness of added layers of InP containing gallium and arsenic—layers anywhere from 20 to 50,000 Å thick. This equipment is crucial in making such an epitaxy process practical in a production environment, and making prices reasonable thanks to high yields. Aimed at fiber-optic telecommunications, the venture's products operate at 1.3 or 1.55 nm. They will include lasers, photodetectors, transmitter and receiver modules, optical switches, and packages that combine silicon chips with optical devices operating at up to 2.4 gigabits/s. □

AUSTRALIAN CACHE CHIP ENTERS KOREAN-OWNED DOOR TO U. S. MARKET

Australia's Austek Microsystems Ltd. will be giving Zymos Corp. a leg up in the market for chip sets aimed at manufacturers of 80386-based personal computers. The Sunnyvale, Calif., company will fabricate and sell Austek's cache controller chip, thereby gaining a big advantage in the high-performance personal-computer segment—machines running at clock rates of 20 MHz and more. Without a cleverly implemented cache memory, such systems get bogged down waiting for their own memory to catch up with them. Zymos claims the A38152 Microcache from the Adelaide-based Austek [*Electronics,* June 11, 1987, p. 74] towers over the competition—especially on price. It sells for $80 in 84-pin plastic leaded chip carriers, compared with $130 to $180 for similar chips in expensive pin-grid arrays. Zymos, which is owned by Daewoo Telecom Corp. of South Korea, will add the chip to its Poach/AT386 line. □

ASIAN COUNTRIES WILL NARROW THE GAP IN MANUFACTURING AUTOMATION

North America will outspend Asia $17.8 billion to $13.8 billion for manufacturing-automation gear this year, but the difference will narrow over the next half decade: the Asians will boost their spending to $22.6 billion by 1991 while the North American market moves to $25.4 billion. Those projections come from David Penning, a manufacturing-automation analyst with Dataquest Inc., San Jose, Calif., after a recent two-week swing through Japan, South Korea, and Taiwan. "There will be more investment in manufacturing automation as a percentage of growth in the Asian countries," he says. So far, Japan dwarfs its neighbors: Dataquest expects the market there to reach $17.1 billion in 1991, compared with $2.1 billion for South Korea and $1.1 billion for Taiwan. But Penning notes that "a lot of people think South Korea is going to be the next economic miracle in the Far East." □

MATRA-HARRIS TO SECOND-SOURCE NEC 16-BIT MICROCOMPUTERS

NEC Corp. is counting on a second-source deal with Matra-Harris Semiconducteurs, Nantes, France, to help ease the friction between European countries and Japan over semiconductor trade. The Tokyo company will provide MHS with the technology to fabricate 16-bit one-chip microcomputers with 8-bit external data buses. The chips—μPD78312 and μPD78310—feature a 16-by-16-bit hardware multiply time of 3.2 μs and a 32-by-16-bit hardware divide time of 8.4 μs. The μPD78312 has an on-chip read-only memory of 8 Kbytes, the μPD78310 has none. NEC has been selling the chips in Japan for some two years. □

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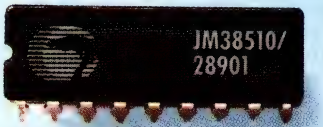

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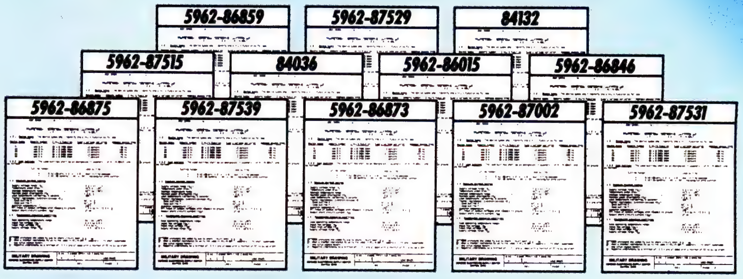

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INTERNATIONAL WEEK

HIGH-CAPACITY LIGHT LINK SET IN JAPAN

Starting next month, NEC Corp. of Tokyo will begin supplying the world's highest-capacity optical-communications system to Nippon Telegraph and Telephone Corp., also of Tokyo. The backbone system will have a capacity of 1.544 gigabits/s, four times the capacity of the current 400-Mbits/s systems installed in Japan. It will link Tokyo and Osaka, and it is scheduled for completion by March 1988.

SAMSUNG, TOSHIBA REACH VCR ACCORD

Samsung Electronics Co., Seoul, will build hi-fi VHS video-cassette recorders using technology from Toshiba Corp., Tokyo. Toshiba says the two firms will sign a formal contract before year's end, and that the pact will be its first technology-transfer agreement in VCR production. Samsung, which now produces about 250,000 VCRs a month, will start manufacturing the hi-fi VCRs next year. Samsung is also negotiating a contract to produce Toshiba-brand hi-fi VCRs for the Japanese company.

EQUIPMENT BUDGET FOR NTT GOES UP

Nippon Telegraph & Telephone Corp. says that during the fiscal year ending in March 1988 it will increase purchases for computer systems to 98.4 billion yen, up from 80.5 billion yen last fiscal year. Without specifying its budget allowances, NTT says it will also purchase other high-tech equipment, including local cable, single-mode optical-fiber cable, digital equipment, single-line telephone sets, desktop coin-operated public telephones, and mobile radio communications equipment. There's an opportunity there for foreign suppliers: last fiscal year, NTT funneled 9% of the 400 billion yen it spent on high-tech equipment to foreign suppliers, mostly in the U. S.

TELECOM FIRMS PAIR UP FOR ISDN

Northern Telecom Ltd. has signed an agreement to purchase for £445 million ITT Corp.'s 24% holding in STC plc, a major British supplier of communications and information systems. STC, in turn, would acquire a 40% interest in the Canadian telecommunications company's British subsidiary. If the purchase of the STC shares is approved by the UK government, the two transactions would enable the companies to jointly develop components for the Integrated Services Digital Network.

EDS TO BUILD SYSTEM FOR ASIAN GAMES

A joint U. S.-Chinese venture will design and develop a $10 million computerized data-management system for the 1990 Asian games in Beijing. The integrated system will be produced by Beijing International Information Processing Co., a joint venture between Electronic Data Systems, of Dallas, and a mainland Chinese group, the Beijing municipal government's Commission for Science and Technology. It will provide the hardware, software, and communications components to cover the 26 major and 240 minor sporting events, coordinating competition results and providing electronic mail, computer-aided sports analyses, and monitoring and control. The system will be installed in the Chinese capital in 1989.

NIXDORF TAKES POS LEAD IN AUSTRALIA

West Germany's Nixdorf Computer AG has become the leading point-of-sale systems supplier to Australia thanks to a Sydney department store. The Paderborn-based Nixdorf nabbed an order from Grace Brothers to deliver some 2,000 computerized cash registers to the department store chain, one of the continent's largest. Nixdorf will be supplying its 8812 system; a Nixdorf 8862 computer at each store will collect the data coming from the cash registers and send it to the chain's computer center in Melbourne.

AEG TO SELL SOLAR PACK TO POWER TV

Will people carry their TV sets to the beaches as they now do their radios? That prospect is closer to reality now that West Germany's AEG AG has come out with a solar-power plant the size of a briefcase, which powers color-TV sets made by Grundig AG, also of West Germany. The Solar Power Pack consists of a solar generator fitted with solar cells delivering a total of 40 W. A solar-charged battery ensures TV reception up to four hours under no-daylight conditions.

SOVIET ORDER FOR IBM 9370 BANNED

Overruling approval by the U. S. Commerce Department, the Defense Department has forbidden IBM Singapore from selling a $250,000 Model 9370 minicomputer to the Singapore Soviet Shipping Co., or Sinsov. Singapore's United Industrial Corp. owns 50% of Sinsov and the Soviet Union the other 50%—a situation that raised Pentagon concerns that the computer might be put to military uses. "Our viewpoint is that Sinsov is owned by the Soviets, and the bottom line is that this line of computers is not for sale to certain countries," says Col. Arnold Williams, U. S. Defense Department spokesman. Sinsov says it wants a computer to process documentation and accounting work for the more than 1,000 Soviet vessels that call yearly at Singapore's harbor, the world's busiest. Instead of the 9370, it will buy a less powerful $125,000 IBM System 36 from a local dealer.

THORN TO SUPPLY AIR DEFENSE AID

Thorn EMI Electro Optics Division of Hayes, England, has won a £70 million contract from the UK Ministry of Defence to supply an Air Defence Alerting Device, which is portable or can be mounted on a vehicle. The device warns ground forces of the presence of low-flying aircraft and helicopters by sensing the infrared emissions of intruding aircraft, then gives their bearing to a weapons operator. It remains undetected itself.

SHARP USES SONY'S 2-IN. DISK DRIVE

Sony Corp.'s 2-in. floppy-disk drive [*Electronics*, Sept. 17, 1987, p. 54E] has found a home in another company's product. Sharp Corp., Tokyo, started marketing a portable Japanese and English word processor that incorporates the drive on Oct. 21. The new word processor, which is equipped with a thermal-transfer printer with a resolution of 24 by 24 dots per character, can also process punctuation and characters for German, French, and Spanish, and incorporates a spelling checker for English-language processing. Sharp expects to sell about 10,000 units a month at 85,000 yen in Japan.

SIEMENS PCs ARE #2 IN GERMANY

West Germany's Siemens AG sold more than 21,000 MS-DOS-based personal computers for professional applications during the last fiscal year, which ended Sept. 30. Combined with its sales of Unix-based machines, those sales push the Munich company to No. 2 in its home market, behind IBM Corp.

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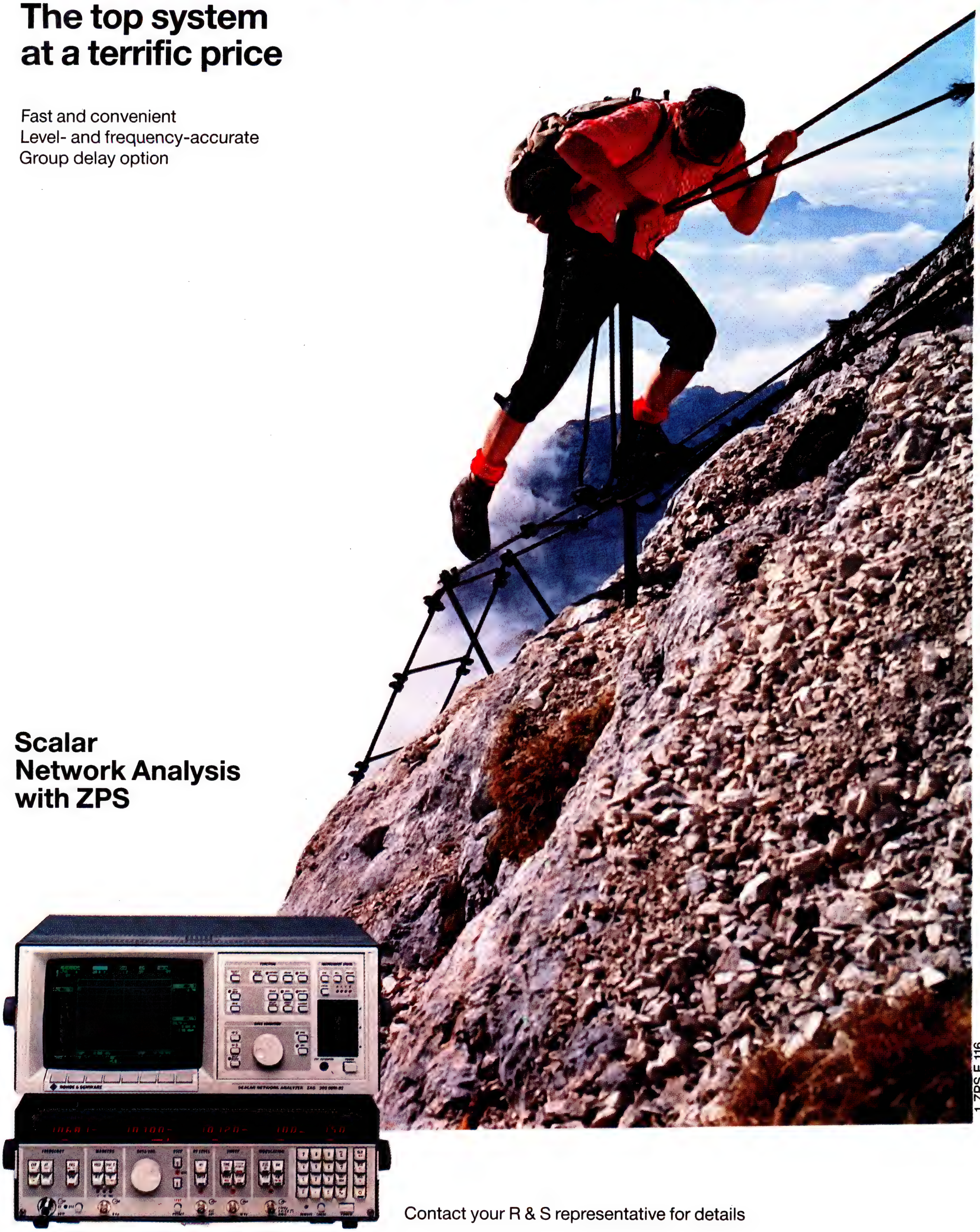

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Circle 98 on reader service card

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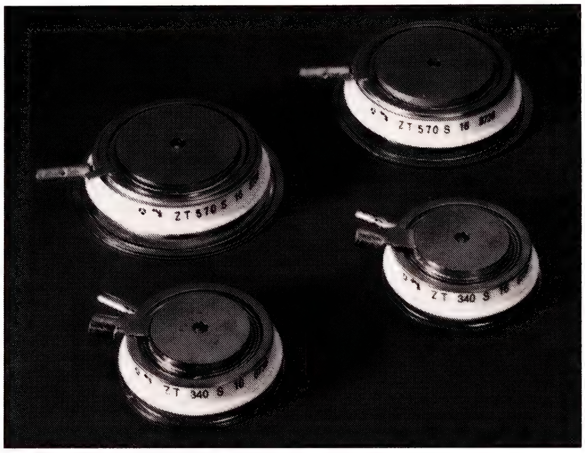
THYRISTORS OPEN NEW VISTAS BY HANDLING 20-KHz SWITCHING

THOMSON'S ZERO-TURN-OFF DEVICES ALSO USE 20% LESS POWER



PAIRS. The ZT340s, front, handle peaks of 500 A at 5 KHz and 400 A at 20 KHz, while ZT570s handle 700 A and 900 A.

A new world of high-power, high-frequency applications in power conversion will open up to thyristors now that Thomson Semiconducteurs is pushing maximum switching frequency from 2 KHz up to 20 KHz in its new ZTO devices that can handle up to 1 MW. ZTOs—the name stands for Zero Turn-Off time—also deliver 20% cost savings over gate-turn-off, or GTO, thyristors, so a wide range of users will benefit from reductions in weight, volume, and cost, says the French chip maker.

Thomson foresees initial applications for ZTOs in resonant converters for induction heating. Future applications include traction, motor-drive, and uninterruptible power supplies. ZTOs will also replace tubes and improve the power range and performance of generators in X-ray, radar, and laser power supplies, says Jean Pierre Abgrall, marketing manager for power devices.

LOW COST. "The cost limitation in all high-power equipment is more the transformers and other passive components, rather than the semiconductors," says Abgrall. "If you today replaced a GTO with a ZTO, your cost for the same amount of output power will be 20% less because you can take more current from the same silicon chip and you will save on passive components."

Until now, high-performance motor-drive techniques with high switching frequencies (10 to 20 KHz) were limited to about 10 to 20 KW because there were no semiconductors capable of handling both high frequency and high power. The turn-off capability of GTOs now being used for applications such as variable motor drives has enabled designers to eliminate commutation networks required by regular thyristors, but GTOs can handle only a limited current during gate switch-off. The GTO also has a dead-time turning switch-off when the device cannot be switched again, and as a result can handle operating frequencies only up to 2 KHz.

To solve these problems, Thomson used a technology based on high interdigitization of gate-cathode junctions. The gate cathode is divided in a great number of cells to accelerate charge extraction at turn-off. To turn off a ZTO, anode current is first forced to zero by a small commutation circuit. Then a negative gate voltage is applied in order to extract stored charge and restore the device's blocking capability almost instantaneously—1 μs or less. In this configuration, no focusing current occurs, which keeps power dissipation low.

The power of the gate drive at turn-off is much smaller than for a GTO because charge extraction from the gate can be implemented with a capacitor of a few microfarads. In a chopper configuration of 1,000 A and 1,000 V, for example, where a conventional fast switching thyristor is used, the extinction capacitor will be 40 μF, and switching frequency will usually be a maximum of a few kilohertz. If a GTO is used, the snubber capacitor requirement drops to 3 μF, but there will be no improvement on frequency. If a ZTO is used, the snubber capacitor will be only 1 μF, and frequency will be limited only by the thermal dissipation capacity of the device, with switching frequencies higher than 20 KHz.

For the moment, Thomson is the only company making the device, but it expects others to begin scrambling to come out with similar products. The world market for high-power components—over 100 A—is around $300 million, with a growth rate of about 5%, says Abgrall. "With these new applications we can expect the market to grow very fast—perhaps 15% for these particular components," he says.

One of the first applications for Thomson's ZTO will be for dc-dc converters aboard the next generation of France's high-speed trains, known as TGVs, for Trains a Grande Vitesse. The present TGVs use regular thyristors and have battery chargers weighing 500 kg. The new ones will use ZTOs and have battery chargers weighing 150 kg.

Until now, high-performance motor drive techniques with high switching frequencies (10 to 20 KHz) were limited to approximately 10 to 20 KW because there were no adequate semiconductors for higher power.

Production will start in Tours in October. Two series of products are now available for sampling, both with blocking voltages up to 1,600 V. The ZT340 series handles currents up to 500 A, and the ZT570 handles up to 900 A. Export prices range from about $200 to $300, respectively, in lots of 1,000.

– Jennifer Schenker

Thomson Semiconducteurs, 43 Ave. de L'Europe, 78140, Vélizy-Villacoublay, France.
Phone: 33-39-46-9719 [Circle 500]

IC PERFORMS AT 0.25 MICROSECONDS

Mitsubishi Electric Corp.'s 7700 series of 16-bit microprocessors use 1.3-μm CMOS technology to achieve instruction-execution times as low as 0.25 μs.

Four models make up the series. The M37700M2FP offer a 0.5-μs execution time and the M37700M2AFP boasts an execution time of 0.25 μs. Both offer 16 Kbytes of read-only memory.

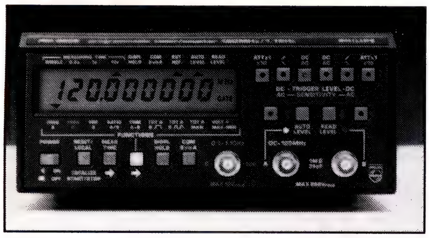
The other two processor chips—the M377002SFP and M37700M2SAFP—offers 0.5- and 0.25-μs execution times respectively. They do not, however, have on-chip ROM.

All four of the chips can access up to 16 Mbytes of memory. All of them target office-automation and industrial-control systems. Available now in Japan, the M37799M2FP costs 2,700 yen; the M37700M2AFP, 3,200 yen; the M37700M2SFP, 2,500 yen; and the M37700M2SAFP, 3,000 yen.

Mitsubishi Electric Corp., Kitaitami Works, Mizuhara 4-1, Itami, Hyogo 664, Japan.
Phone 81-727-82-5131 [Circle 701]

NUMBER GENERATOR BOOSTS SECURITY

The MicroSeal security device from Encrypta Electronics Ltd. indicates if someone has tampered with a computer or peripheral cabinet by automatically generating a random four-digit number that is displayed on the unit's liquid-crystal display.



Measuring 50 by 45 by 15 mm, MicroSeal comes encapsulated in resin and includes a lithium battery that guarantees a 10-year useable life. Besides generating a random number, it also records and displays the time and date when the cabinet was last opened and closed.

Priced at £50 with volume discounts available, MicroSeal is available now.

Encrypta Electronics Ltd., The Bulmore, Caerleon, Gwent NP6 1QR, UK.
Phone 44-633-423-511 [Circle 702]

TIMER IS PROGRAMMED OVER RS-422 BUS

The PM6666 timer/counter from Philips offers full programmability over the RS-422 bus, including input settings, trigger levels, and sensitivity. Up to 20 measuring functions including voltage minimums and maximums can be selected remotely over the bus. Automatic triggering is supported for input signals over 100 Hz with trigger voltage levels ranging from +50 to –50 V at a resolution of 20 mV.

Trigger levels can be displayed on the instrument's screen, and three-state light-emitting-diode indicators give an instantaneous indication of triggering inputs. Sensitivity can be set at any of six levels ranging from 20 mV to 1 V.

The instrument offers seven-digit frequency-measurement resolution. The PM6666 is available now, with the price varying from country to country.

Philips Industrial & Electro-acoustical Systems Div., P. O. Box 218, 5600 MD Eindhoven, The Netherlands.
Phone 31-40-788620 [Circle 703]

TELECOM UNIT MIXES VOICE AND DATA

Standard twisted-pair telephone lines can simultaneously carry both data and voice traffic with the TAD XD integrated services module from Datentechnik Ltd. Capable of transmitting synchronous or asynchronous data at speeds up to 19.2 Kbits/s, the TAD XD can be used on cabling runs as long as 10 km within the user's premises.

The module provides basic services similar to the emerging Integrated Services Digital Network standard without requiring new terminal equipment and local-loop cabling. It can also be used to provide value-added services such as high-speed videotex or access to packet-switching networks. It is available now, and price varies by country.

Datentechnik International Ltd., Communications House, 51a Heathhill Rd., Crowthorne, Berks RG11 7BP, UK.
Phone 44-344-779-398 [Circle 704]

JITTER METER RUNS UP TO 168 MBITS/S

The PJM-4 jitter meter from Wandel & Goltermann handles signals with frequencies up to 168 Mbits/s on digital transmission networks. It measures a wide range of bit rates, weighting types, and interface codes, and can tackle the numerous system interfaces encountered in line-radio-link and optical transmission systems.

To determine the effects of jitter on overall transmission quality, the PJM-4 counts the number of times that certain adjustable jitter thresholds are exceeded in the course of continuous measurements. Signal-code violations are counted at the same time.

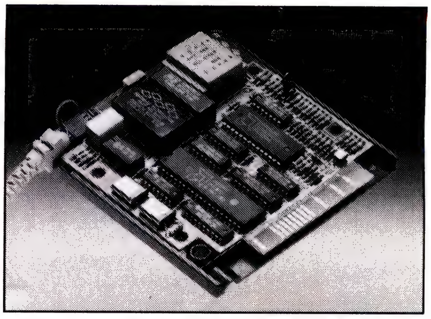
Price for the PJM-4, which can now be delivered, depends on importing country.

Wandel & Goltermann GmbH, P. O. Box 45, D-7412 Eningen, West Germany.
Phone 49-7121-891570 [Circle 705]

REED SWITCH OFFERS 4,000-V ISOLATION

A miniature reed relay from Gentech Ltd. provides modem interfacing of phone lines with computer peripherals where high isolation between switched circuits and coil drive circuitry is vital. The G32V provides 4,240 V dc coil/contact isolation and comes in either dry or mercury-wetted versions.

Both versions can be customized. The relays are fully encapsulated and are available in 5-, 12-, and 24-V models. They are available now. Price depends on importing country.



Gentech International Ltd., Grangestone Industrial Estate, Girvan, Ayrshire, Scotland KA26 9PS, UK.
Phone 44-Girvan 3581 [Circle 706]

GRAPHICS CARD RUNS 640-BY-480 DISPLAY

The VME 68800 color graphics board from BICC-Vero Electronics Ltd. offers 640-by-480-pixel resolution, and a 30.24-MHz display speed. The standard version comes with 256 Kbytes of dual-port video random-access memory and a 16-color palette.

The VMEbus board includes a complete OS-9/68000 software driver and supports a 60-Hz frame rate. With an optional video-RAM expansion to 512 Kbytes, it provides 1,024-by-1,024-pixel resolution and vector drawing up to 64 million pixels/s. An optional color palette provides up to 4,096 colors.

The OS-9 software driver supports four fonts for ASCII display and graphics routines for drawing lines and filling regions with color, textures and patterns. Available now, the board costs £450.

BICC-Vero Electronics Ltd., Flanders Road, Hedge End, Southampton SO3 3LG, UK.
Phone 44-703-266-300 [Circle 707]

RAM BOARD BOASTS DOUBLE PROTECTION

Xcalibur Computers Ltd.'s RAM-BO battery-operated static random-access-memory board for IBM Corp. Personal Computers and compatibles offers a maximum capacity of 1 Mbyte and two independent batteries to guard against power failures.

The board is designed for use in environments where dust, noise, and vibration make rotating storage devices such as disk drives unreliable. The batteries boast 10-year operating lifetimes. Target applications include data logging, industrial control, and image capture and analysis. Access time varies depending on the host computer.

Variable amounts of RAM are available and one version comes with 500

BOUT THE REPRODUCIBILITY OF TOSHIBA ATE ARRAYS.

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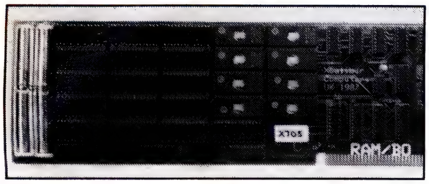


Kbytes of RAM and 500 Kbytes of erasable, programmable read-only memory Available now, the standard board with 500 Kbytes of RAM costs £399.

Xcalibur Computers Ltd., Kent House, 30 Billing Rd., Northampton NN1 5DQ, UK.
Phone 44-604-259-211 [Circle 708]

OPTICAL MULTIPLEXER HANDLES 3 SIGNALS

The HK-1300 optical-waveguide multiplexer/demultiplexer from Shimadzu Corp. combines or separates up to three signals with wavelengths of 1,200, 1,310, and 1,550 nm.

The unit incorporates an optical-waveguide and defraction-grating technology to achieve its multiplexing/demultiplexing functions. Since all parts are integrated into a single module, the HK-1300 is moisture-proof.

Operating temperature range is –10 to +55°C, and minimum insertion loss is 5 dB. Available now, with delivery within two to three months after order, the HK-1300 costs 300,000 yen.

Shimadzu Corp., Opto-electronics Dept., Shinjuku Mitsui Building, 2-1-1 Nishi Shinjuku, Shinjuku-ku, Tokyo 163, Japan.
Phone 81-3-346-5556 [Circle 709]

PC-BOARD FAB SYSTEM IS SELF-CONTAINED

Two systems from Mega Electronics Ltd. offer self-contained operation with three process tanks for the development, bubble-etching, and immersion-tinning processes for production of printed-circuit boards.

The PB510 system handles 12-by-10-in. boards, and the PB520 system, 20-by-12-in. boards. Positioned between the three process tanks are two spray-wash tanks. The three process tanks have a built-in hose and tank to simplify maintenance, and each spray-and-wash tank has its own water inlet.

The systems are available now; prices start at £820.

Mega Electronics Ltd., 9 Radwinter Rd., Saffron Walden, Essex CB11 3HU, UK.
Phone 44-799-21918 [Circle 710]

SIGNAL GENERATORS ACCURATE TO 1 mHZ

The model 1049 sine-wave and noise generator and the 1051 sine-wave generator from Bruel & Kjaer handle frequencies from 2 to 200 KHz with a resolution of 1 mHz.

Output levels range from 100 μV to 5 V and are selectable with an attenuator accuracy of ±3 dB. Output signal distortion is better than –96 dB in the audio range and is typically –105 dB at a frequency of 1 KHz.

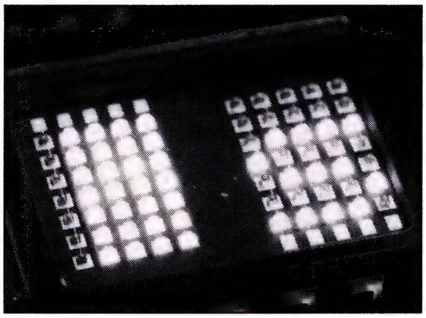
For frequently repeated tests, the instruments offer nine programmable pattern settings.

Other features include narrow-band random-, white- and pink-noise outputs and a compressor that maintains a constant output signal. The instruments are available now. Price depends on importing country.

Bruel & Kjaer, 18, Naerum Hovedgade, DK-2850 Naerum, Denmark
Phone 45-02-800-500 [Circle 713]

DOT-MATRIX DISPLAYS OPERATE TO 85° C

Siemens AG's PD 3535 (orange) and PD 3537 (green) dot-matrix displays offer an operating range of from –40 to +85°C and a humidity limit of 85% at 85°C. The 5-by-7-dot matrices are 7 mm high. Brightness, flashing, erasing, and a test program for the message to be displayed are all controlled by CMOS and bipolar circuitry within the four-pin package.



The chips' programmability saves users from having to provide a character generator, multiplex oscillator, and driver circuits. Up to seven of the units can be aligned without additional circuitry and other overhead.

Viewing angle is ±55° on the x axis and ±65 on the y axis. Price depends on importing country.

Siemens AG, P. O. Box 103, D-8000, Munich 2, West Germany.
Phone 49-89-2341 [Circle 711]

DATA MONITOR STORES UP TO 8,000 READINGS

Mors Components' 8-bit Data Acquisition System handles both digital and analog inputs and stores up to 8,000 measurements. Acquisition times can be set from 1 s to 1 hour.

Typical applications include storing electrical measurements, thermocouple readings, and moisture data. An internal power supply allows the DAS to run in standalone mode for up to six months.

The unit can be interfaced with Seiko-Epson Corp.'s HX 20 personal computer and IBM Corp.'s Personal Computer.

Available now, the unit's price depends on importing country.

Mors Automatismes Industriels, Centre d'Affaires Prisnord, Tour Ampere, 93155 Le Blanc Mesnil, France.
Phone 33-48-65-33-23 [Circle 712]

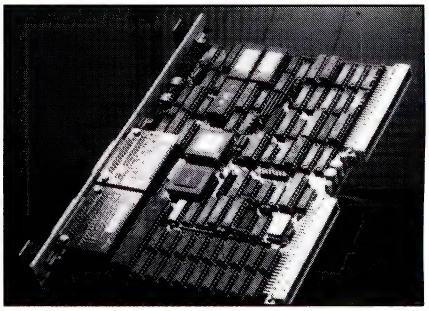
X.25 TELECOM BOARD DOES 400 PACKETS/S

Thomson Microsystems' new TSVME 541 dual-channel communications controller board for CCITT X.25 packet switching achieves a data transfer rate of 400 packets/s on 64-Kbit/s transmission lines. Up to 62 virtual circuits can be supported. The board is compatible with the VMEbus standard, which suits it for industrial applications.

Based on Motorola Inc.'s 68010 microprocessor, the board offers 512 Kbytes of dual-port random-access memory with parity check. The TSVME 541 also has direct-memory-access capability in two high-level communications links.

The board's 68450 DMA controller features four channels with a 4-Mbyte/s access rate. The 68464 SIO controller has two channels that can be used in synchronous mode. The board is available now. Price depends on importing country.

Thomson Microsystems, 66 rue du Fossé Blanc, BP 156, 92231 Gennevilliers Cedex, France.
Phone 33-1-47-90-64-00 [Circle 715]



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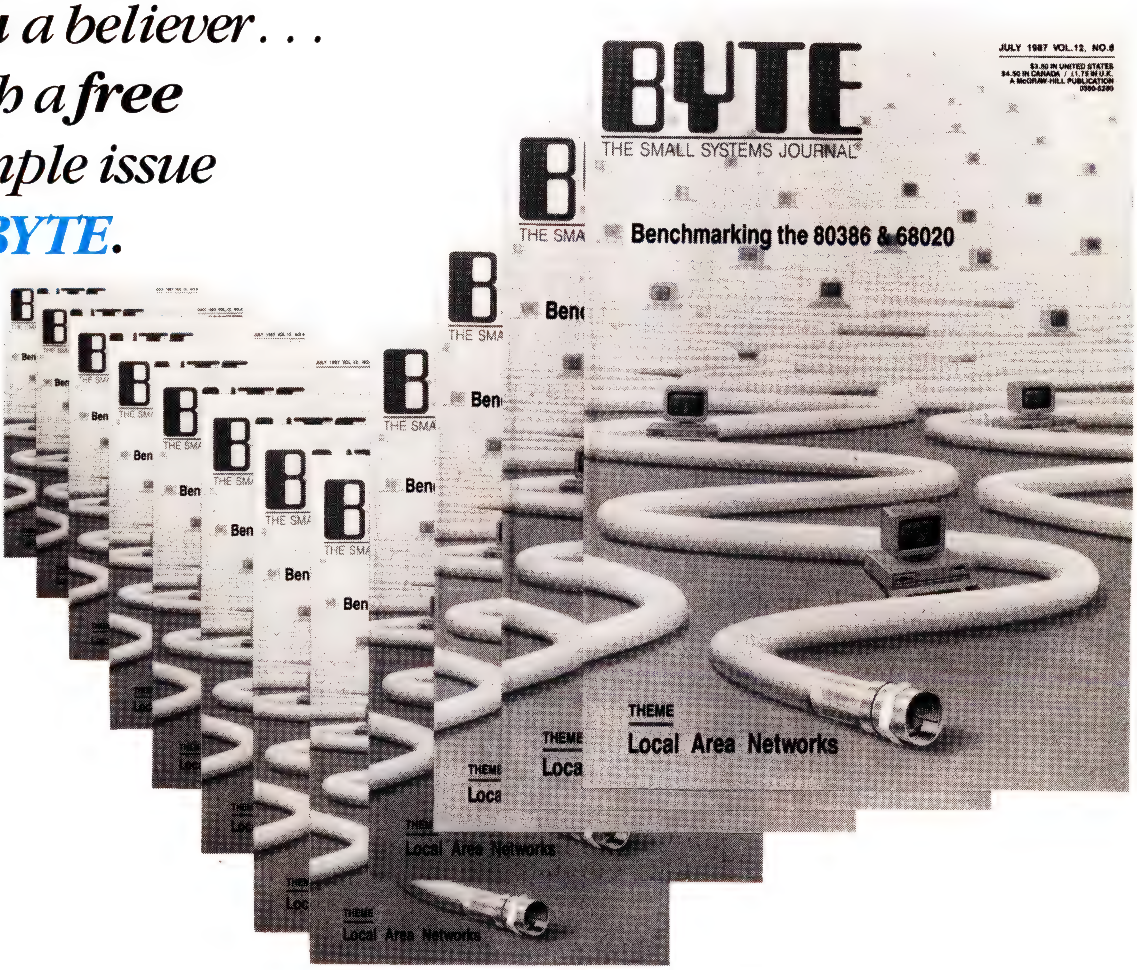
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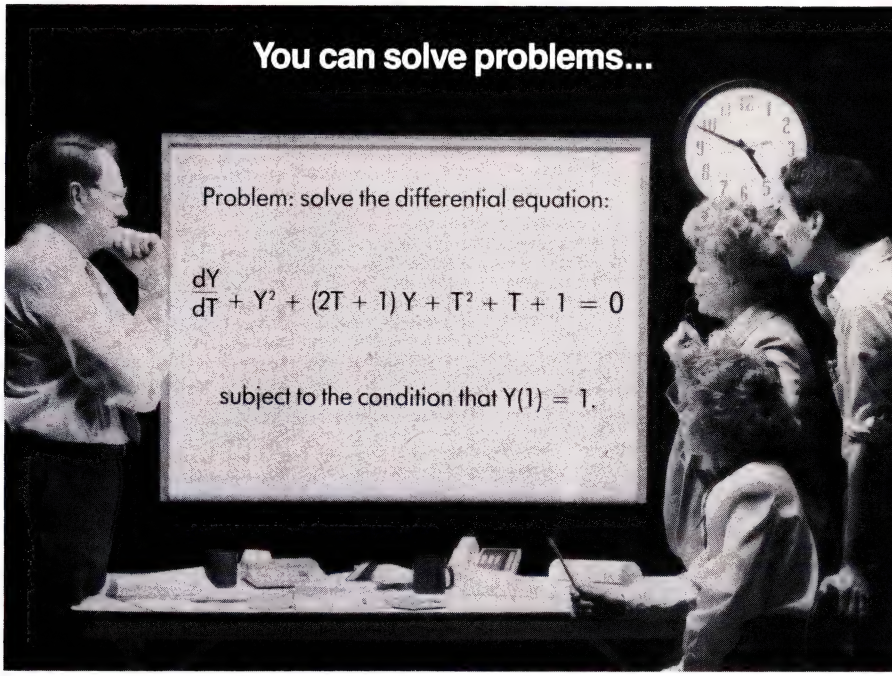

Problem: solve the differential equation:

$$\frac{dY}{dT} + Y^2 + (2T + 1)\,Y + T^2 + T + 1 = 0$$

subject to the condition that Y(1) = 1.

Symbolically...

```
(C1) DEPENDS(Y,T)$
(C2) DIFF (Y,T)+Y^2+(2*T+1)*Y+T^2+T+1;
      dY     2                   2
(D2)  -- + Y  + (2 T + 1) Y + T  + T + 1
      dT
(C3) SOLN:ODE(D2,Y,T);
                    T
            %C T %E  - T - 1
(D3)  Y = - ----------------
                    T
              %C %E  - 1
(C4) SOLVE(SUBST([Y=1,T=1],D3),%C),NUMER;
(D4)    [%C = 0.5518192]
(C5) SPECIFIC_SOLN:SUBST(D4,SOLN);
                          T
            0.5518192 T %E  - T - 1
(D5) Y = -  -----------------------
                         T
              0.5518192 %E  - 1
```

and Numerically.

```
(C6)  FORTRAN(D5)$
       Y = -(0.5518192*T*EXP(T)-T-1)
   1       /(0.5518192*EXP(T)-1)
```

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PROBING THE NEWS

LSI LOGIC'S GIANT ARRAY BREAKS THE RECORD FOR USABLE GATES

ITS 100,000-GATE CHIP IS FIRST OF A NEW GENERATION COMING

by J. Robert Lineback

MILPITAS, CALIF.

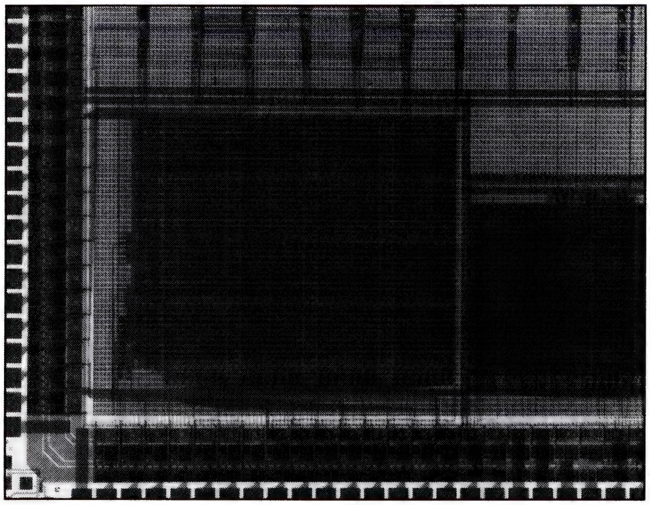
Make room for some big new gate arrays. Better make plenty of room—LSI Logic Corp. is shoving the density barrier of commercial arrays out to a whopping 100,000 usable gates. The company's new arrays are fabricated with a new 1-μm, triple-level-metal CMOS process packing a million transistors onto a single 1.5-by-1.5-cm chip.

LSI Logic's new LCA100K Compacted Array Plus family promises to deliver huge semicustom designs from a channelless sea of 236,880 total gates. That kind of size is catching other suppliers and some customers by surprise. It significantly raises the gate-count stakes in application-specific integrated circuits by nudging mask-programmed logic arrays into territory that once was the secure turf of standard-cell ASICs.

The Milpitas-based company is first out of the chute with 100,000 usable gates, but competing suppliers like Motorola, VLSI Technology, and NEC are preparing their own large CMOS arrays. Clearly such big arrays bring an ASIC company added prestige, but some observers question their usefulness. They say that density level is better served by standard-cell ASICs and compiled designs. LSI Logic and others, however, see a real market, especially in the high-end computer markets. As they refine their technology they are likely to offer arrays that are larger still.

Huge gate arrays, however, face some serious obstacles. Most test equipment can't handle them, some design tools need to be improved, and major strides in packaging technology are needed to accommodate their big pad counts. Some observers wonder who's going to use them, and for what.

LSI Logic thinks the availability of 100,000 usable gates on a quickly customizable logic array will quickly be embraced by the traditional users of 50,000-gate CMOS devices, says Gerald S. Rau, product marketing manager for advanced logic arrays. Those devices are being used mostly to build central processing units for supermini, mainframe, and minisupercomputer systems (see p. 56). The big new payoff, Rau predicts, is likely to come in several emerging areas, such as parallel processing, and in new real-time computing markets, such as signal processing, which now have no hardwired options for algorithms bogged down in software.



BIG ONE. LSI Logic is headed for production with a sea of 236,880 gates, of which 100,000 can be used. One ninth of its area is shown.

With the high gate densities, Rau expects to see software-embedded algorithms hardwired for greater speed in image processing, artificial intelligence, speech recognition, and high-resolution computer graphics. In addition, the fast turnaround and lower nonrecurring engineering costs of large gate arrays compared with standard-cell ASICs should make the new Compacted Array Plus series popular with system designers who want quick complex prototypes, packed with dense on-chip memory.

Showing no doubt that a market will emerge, LSI Logic is working hard on the technology that large gate arrays require. The Compacted Array Plus family is being introduced with three master slices of 139,104 to 236,880 total raw gates. It offers a 20% speed improvement over the two-year-old LCA100000 series of 1.5-μm, double-level-metal CMOS arrays with up to 50,000 usable gates out of 129,042. The 1-μm, triple-metal LCA100K family has internal propagation delays of 460 ps for a 2-input NAND at 25°C. The new family is based on the same LSI Logic master-slice Channel-Free architecture as the firm's current series. Its increased performance, density, and gate-routing capabilities are due to the process shrink from 1.5 to 1 μm and the addition of a third level of metal.

LSI Logic's channelless architecture forms gates with four transistors placed together, isolated from other gates by oxide. The company says the scheme provides higher density than other transistor-isolation approaches allow, because the oxide is only 1/7th the width of a transistor. Also, Rau says the grouping of four transistors is an ideal structure for implementing memory on the logic array. The densest LCA100K chip, he says, can carry 16 Kbits of 15-ns random-access memory, 64 Kbits of read-only memory, and 46,000 gates of usable logic. A key development in the process shrink has been the reduction of metal pitch, says Rau, who declines to disclose the measurement between interconnect-line centers.

Motorola Inc. is right on LSI Logic's heels. It is expected to introduce in November a new triple-metal family of CMOS high-density arrays, called the HDC series. The HDC family will offer greater gate-utilization rates—approaching 80%, compared with 40% for LSI Logic's new series—delivering up to 80,000 usable gates from a 483-by-483-mil master of only 104,832 total gates. And Motorola plans arrays supporting more than 100,000 usable gates.

In Carrollton, Texas, Thomson Components-Mostek Corp. is considering adding a third layer of metal to its recently introduced double-level-metal 12000-series CMOS channelless arrays [*Electronics*, Aug. 20, 1987, p. 42]. The third layer could push the usable gates of a total of 128,000 from about 50% to almost 90%, near the 100,000 level. Also expected to push semicustom CMOS arrays to and beyond 100,000 usable gates are such Japanese powerhouses as Toshiba, Fujitsu, and NEC.

NEC, unlike most American suppliers, is planning to serve the high end with a channeled array, stacking layers of metal interconnection atop each other for high utilization. NEC will move into the 50,000-gate range in November with the introduction of a 1.2-µm triple-level-metal CMOS-V product line. The company is considering fabricating four or even five layers of metal interconnection in its push towards 100,000 gates.

At Honeywell Inc.'s Digital Technologies Center in Colorado Springs, Colo., a next-generation submicron combined bipolar-CMOS technology is being prepared for a new line of military-targeted arrays with densities in excess of 100,000 usable gates. "What you are really buying with 100,000 gates is the ability to put more of a subsystem on a chip. Today, with 50,000 gates, we are talking about subsystems like CPUs and signal processors. By going to higher densities you begin adding memory" and data-path circuits, says David Bondurant, CMOS product line manager.

At least one observer sees some marketeering in the rush to huge arrays. "The largest market reality is the customer perception, and in the ASIC buyer's perception, you must offer the most advanced product to be considered a viable vendor," says Dean A. Winkelmann, semicustom-chip analyst at Integrated Circuit Engineering Corp. in Scottsdale, Ariz. Winkelmann is skeptical about the 100,000-usable-gate market potential, believing the market for ultra-large gate arrays will grow smaller as densities increase. He points out that standard-cell chips are both faster and smaller.

Texas Instruments Inc. in Dallas is interested in delivering 100,000-gate density to ASIC markets, but "we continue to question the viability of gate-array structures for that kind of complexity," says Douglas S. Rasor, marketing manager for ASICs. "For super-dense, complex designs, we feel that customization of all levels of a chip will be the only way to achieve the die size that is necessary for yielding well in production. Reliability also comes into question when you get above 250 and 300 mil^2."

'100,000 gates might seem a bit outrageous now, but not in 5 years'

On the other hand, "over the next five years, I don't think 100,000 used gates will be that unrealistic," says Bryan Lewis, a researcher at Dataquest Inc., San Jose, Calif., who follows the semicustom array market. "It might sound a bit outrageous now, but not in five years," he says.

In fact, the increasing size and packing densities of new arrays is changing the rules of the game, say executives at VLSI Technology Inc., San Jose, Calif. The company serves the market for 100,000-gate plus designs with cell-based ASICs and compiled designs, which offer densities approaching hand-packed levels. "VLSI Technology is recognizing that there are some ingrained market positions that want the [fast] turnaround of gate arrays," says James Ulagowski, manager of advanced product ASIC marketing. He suggests that the rising densities of new array architectures and triple-level metal are biting into the standard-cell market.

So VLSI Technology is moving to add dense gate arrays to their product line: it plans to announce high-density channelless arrays, most likely in early spring. The arrays are expected to be in the same density range as LSI Logic's new family.

Meanwhile, LSI Logic continues to run testing prototypes based on the new arrays in its new 6-in. wafer facility in Milpitas while waiting for customer designs, which are expected by mid-1988. The cost of most of those parts will range between hundreds of dollars and thousands, depending upon complexity and volumes. Power dissipation is initially being quoted at 12-µW/MHz per gate, about the same as the older 1.5-µm family, which covers a range of 10,000 to 50,000 usable gates.

LSI Logic is aiming much of the development work now at testing techniques and high-pin-count packages. The company has built boundary-scan testing into its products to speed up post-production testing. It also has a proprietary circuit option aimed at speeding test times. Its arrays offer up to 364 device pads, of which initially only 256 input/output signals will be made available because of test-equipment limitations. LSI Logic plans to increase the available I/O pins with the arrival of new testing gear, and hopes that tape-automated bonding techniques will make packages possible that support its arrays' high pin counts.

In fact, available pins is the biggest issue facing many system designers, says Ronald Bernal, director of advanced development at Edge Computer, Scottsdale, Ariz. "For us, the pin count is No. 1, and higher density is No. 2." □

FOR 'DENSITY PIGS,' THE BIGGER THE GATE ARRAY, THE BETTER

The prospect of arrays with 100,000 usable gates might make some heads spin, but it's just the thing that will make some potential users dream of still higher densities. Among advanced scientific computer makers, for example, "we are all pretty much density pigs, if you will," says Harold Dozier, manager of ASIC development at Convex Computer Corp. of Richardson, Texas.

Others heartily agree. They welcome the era of 100,000-gate arrays and expect far more in the future. ETA Systems Inc., St. Paul, Minn., is counting on CMOS arrays in the 100,000-to-200,000-gate range to produce a successor to the ETA^{10}, which is based on 20,000-gate chips from Honeywell Inc.

LSI Logic executives in Milpitas, Calif., say the response has been overwhelming to the promise of routing 100,000 gates on its new logic arrays. Users are considering a range of designs, among them replacing analog portions of signal-processing systems, advanced cache-memory schemes, increased parallel processing, and hardwiring software-based algorithms for real-time computing.

"We like gate arrays because of the short design cycles [compared to standard cell-based offerings]," says Convex's Dozier, noting the heavy demand upon his design group. He adds that gate arrays tend to stay at the leading edge of processing. "You might find you get nearly the same performance and density from leading-edge gate arrays as you can with standard cell products," Dozier believes.

Still, some computer makers are turning towards standard-cell designs after entering the market with gate-array-based processors. "We design a lot of gate-array products, but I question whether we will stay on that path in the future because of the performance advantage [of more tightly packed standard-cell ASICs]. To me it is not a question of the number of gates, but how much memory you can pack onto a chip," says Ronald Bernal, director of advanced development at Edge Computer in Scottsdale, Ariz. Bernal says the key factor for a system house in choosing between arrays and cell-based designs is deciding whether it wants to acquire in-house the chip expertise it will need to deal with foundry and cell-library issues.

HOW THOMSON AIMS TO BUILD A WORLD-CLASS TV BUSINESS

BUT THE JAPANESE COULD UPSET THOSE PLANS WITH HDTV

by Jennifer Schenker

PARIS

Thomson SA is staking its future on a massive effort to build a world-class consumer-electronics business. On top of a spate of purchases that culminated this summer in the acquisition of General Electric Co.'s consumer electronics operations, the French government-owned company has now decided to invest $3.28 billion over the next 10 years to build up this business. That investment should help Thomson to compete as a world player, but it will by no means guarantee success.

Thanks to its acquisitions, consumer operations already account for most of Thomson's sales (see chart). The company, in fact, is now the world's leading seller of TV sets. But this leadership in TV could disappear almost as fast as it was acquired. The French company faces formidable competition from Japan's TV makers, who are now pushing hard to establish themselves in the next generation of television technology, high-definition TV.

If the Japanese are successful in this drive, it could spell disaster for Thomson's well-laid plans. The Japanese version of HDTV is incompatible both with the TV sets Thomson now makes and with the HDTV technology that it is pursuing (see p. 58). Company president Alain Gomez is well aware of the problem. He sees the Japanese as capable of doing in TV what they've already done in video-cassette recorders: Far Eastern manufacturers now supply 90% of all VCRs sold in the world. Gomez says outright that if that happens in color TV, the heart of Thomson's consumer business, the company could be wiped out completely.

To fight off the Japanese, industry observers believe that Thomson must devote a significant amount of its resources in the next few years to research and development. Focused R&D, they say, should be able to keep the company from being locked out of the emerging HDTV market and help it establish a position in other markets.

At the same time, however, Thomson has to learn the consumer business and consolidate its acquisitions fast. A year ago, most of its sales and expertise were in the defense electronics marketplace. The Japanese, on the other hand, are masters of the worldwide consumer electronics business and will put on a full court press to gain market share. Thomson's consumer operations currently are just a collection of laboratories, plants, and offices scattered around the world, run until recently by a bunch of separate companies. Thomson needs to meld them into a smoothly running global operation.

"Thomson got where it is entirely through acquisitions. They don't have a single identity," says Jim Bottoms, a London-based analyst for Business Intelligent Systems Mackintosh, an international consulting firm. "Everybody knows Sony and Toshiba, and to a slightly lesser extent Philips, but Thomson is unknown by its own name in Britain and the U. S. It is going to have to start moving towards a world identity."

Doing that won't be easy. Thomson started buying other companies in 1974, acquiring GE's consumer electronics operations in Spain. Between 1978 and 1983, it bought four West German companies: the TV makers Normende, Saba, and Telefunken, and an audio firm, Dual. Then, in July, Thomson made its largest acquisition, buying the consumer-electronics division of GE in the U. S., including what had been RCA's consumer operations. Along with the acquisition of that same month of Ferguson in the UK, the deal made Thomson No. 1 in world television sales [*Electronics*, Aug. 6, 1987, p. 32]. The GE/RCA acquisition gave Thomson factories in the U. S. and the Far East, and the biggest marketing and manufacturing facilities on three continents. GE/RCA's color-TV market shares are 24% in the U. S. and 18% in Europe, according to BIS Mackintosh.

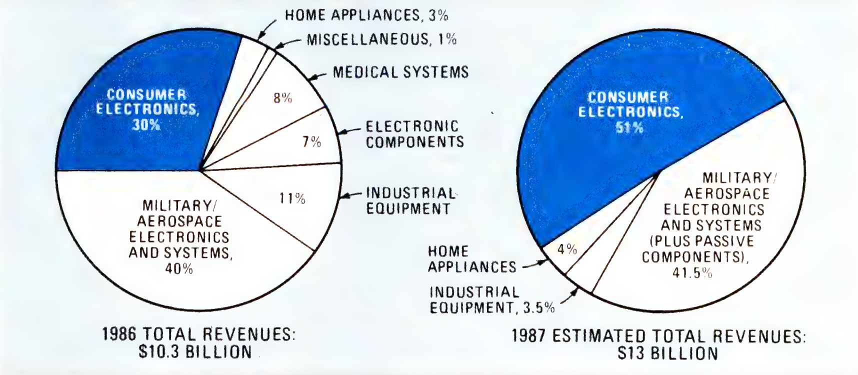
Thomson now projects its total 1987 sales as being $13 billion. Some $7 billion, or 55%, will come from the consumer electronics division, which includes home appliances like microwaves. Last year, the company's total sales were $10.3 billion, and consumer products, including home appliances, accounted for only 33%. Some 40% of sales were in the military/aerospace sector. Components, medical equipment, and industrial products added another 27%.

In 1986, Thomson, GE/RCA, and Ferguson sold $6.3 billion worth of consumer electronics, according to Bottoms of BIS Mackintosh, most of it based on TV equipment. Of the combined total, TV sets represented 61%, VCRs 30%, cathode-ray tubes 3%, and audio and TV components other than CRTs about 6%.

To compete with the Japanese, says Thomson president Gomez, the company will have to concentrate its investment dollars on TV sets, as well as CRTs, VCRs, and audio equipment. For now, the emphasis is on HDTV.

As proposed by the Japanese, HDTV would require new sets, new broadcast equipment, and new channel allocations. The Japanese are ahead of Europe and

THOMSON BETS HEAVILY ON CONSUMER ELECTRONICS



NOTE: 1987 REVENUES DO NOT INCLUDE SEMICONDUCTORS (ACTIVITY TRANSFERRED TO SGS-THOMSON MICROELECTRONICS) AND MEDICAL EQUIPMENT (DIVISION SOLD TO GENERAL ELECTRIC). SOME INDUSTRIAL EQUIPMENT BUSINESSES HAVE BEEN SOLD AS WELL.

FUTURE TV. Thomson's Caillot says the company will be ready for new TV standards.

the U. S. in their HDTV development work, but a major effort is under way to develop a European standard, and the U. S. may adopt a standard of its own.

Thomson is already moving in HDTV. Along with Philips of the Netherlands, the company has been a leader in backing the D2MAC European standard for direct satellite TV broadcasts, as well as HDMAC, says Jean Caillot, president of Thomson International. HDMAC is a metamorphosis of D2MAC planned over the next 10 years that will offer image quality similar to that of Japan's HDTV.

COMPATIBLE. And, thanks to the GE/RCA acquisition, Thomson is getting access to new Advanced Compatible TV technology. Caillot says, "ACTV is necessary to have a norm compatible with existing standards." Unlike the Japanese HDTV, ACTV is compatible with current TV sets and channel allocations.

However, RCA's work on digital TV technology has been moving along slowly. Thomson is not ready to compete directly with the Japanese in improved-definition TV, for example. IDTV uses digital techniques to improve picture quality substantially, using the same TV signal now standard in the U. S. and Japan. Japanese set makers may start selling IDTV sets next year.

Thomson is taking HDTV more seriously than the need for IDTV sets for the U. S. market. Research for HDTV and other areas is vital for Thomson, believes BIS Mackintosh's Bottoms. "R&D is critical. It's something the Japanese spend an awful lot of money on and that Philips spends a lot of money on," he says. During 1984, Philips spent 7% of its sales revenue and Hitachi about 5% of its sales revenue on R&D. "As a world player, Thomson has got to substantially increase its commitment, too," Bottoms says.

Thomson spent a total of $83 million on consumer electronics R&D in 1986, according to its 1986 annual report. That was less than it spent on consumer production facilities—$89 million—but the emphasis that has been placed on production investment over the last two years will be progresssively replaced by R&D, mainly for HDTV, said Renee-Claire Bloch-Gani, a consumer electronics consultant for the Bureau d'Informations et de Prévisions Economiques, a government-supported forecasting organization based near Paris.

However, this month's announcement of the planned $3.28 billion investment is not proportionally any more than Thomson's competitors will spend, Bottoms points out. He figures that if last year's annual sales by GE/RCA, Thomson, and Ferguson remain at about $6 billion over the next 10 years, the planned investment comes to about 6% of their revenue.

And it's not as if Thomson can concentrate all its R&D on HDTV. It needs to advance elsewhere in consumer electronics, too. "If Thomson wants to make its mark, it must get more active in developments that will impact the future consumer components market," an executive at a German components maker says. He mentions interactive compact disks (being developed by Philips) and digital VCRs as examples. So far, Thomson has not stood out in such fields.

Besides the 10-year investment, Thomson is taking other steps to bolster its R&D. New R&D facilities are being set up in Strasbourg, France, and in Singapore, the latter to exploit the consumer electronics expertise available in the Far East. And the acquisitions of the past few years have added their share to Thomson's capabilities—R&D labs were part of the package, for example, when Thomson bought Telefunken and Saba.

However, growth by acquisition offers as many drawbacks as advantages. In GE/RCA's case, the situation is complicated by the fact that RCA has now been acquired twice since 1985; GE had bought it less than two years before selling the combined GE/RCA consumer operation to Thomson. "Thomson's going to have to do a lot of promotion to make up for lost time," says David Lachenbruch, editorial director of *Television Digest* in New York. He singles out management as a problem; most of the executives at RCA left when GE bought it, he says. Lachenbruch thinks Thomson is going to have to work hard to make the organization effective again.

LOST SHARE. He also points out that any TV brand loses market share when its maker is acquired. Thomson already has had to contend with loss of market share with its other acquisitions. In Germany, for example, Thomson now owns less of the market with the combined Telefunken, Nordmende, and Saba than the total share the three commanded as separate companies. As one industry analyst points out, three salesmen from three companies together produce more sales than one salesman representing three separate brand names.

The real test for Thomson, though, is whether it can run an organization of the scale its consumer business has grown to in recent years. The industry analyst, for one, isn't sure it can. "They don't have the decades-long experience that Philips has," he says. But he adds that Thomson has shown signs of flexible, international-type thinking, which might indicate the company is heading in the right direction. "If Thomson continues to show such flexibility, and if it develops the ability to adapt to world conditions, then the firm may well become a major player on consumer electronics markets." ☐

THE DRIVE FOR A EUROPEAN ALTERNATIVE TO HDTV

Thomson SA has teamed up with competitor Philips of the Netherlands, Robert Bosch GmbH of West Germany, and the Thorn EMI research lab in the UK under the umbrella of Eureka, the European research program, to create an alternative to the high-definition television standard proposed by the Japanese.

The four companies are working with the European Economic Commission and a large number of public and private organizations to develop standards for HDTV built around a 50-Hz scan rate, instead of the 60 Hz of the Japanese standard. A proposal is slated to be presented at an International Radio Consultative Committee meeting in 1990.

"The European governments have very strongly agreed amongst themselves and they are in direct opposition to what is being proposed at the moment by the Japanese," says Eamon Lalor, head of the audiovisual division of the EEC's Telecommunications Industry and Innovation sector in Brussels.

"Instead of throwing some 600 million televisions in the trash can, we are advocating an approach that is compatible with existing standards," says Jean Caillot, president of Thomson International. Thomson has poured money into the joint project, which backs the D2MAC standard for direct satellite TV broadcasts and its evolution into the HDMAC (high-definition) standard.

The European system features hi-fi stereophonic sound, multichannel sound, a data channel for subtitles, teletext, and remote computer access. It will also provide a better picture, wide-screen displays compatible with film, and double the number of scan lines, to over 1,000.

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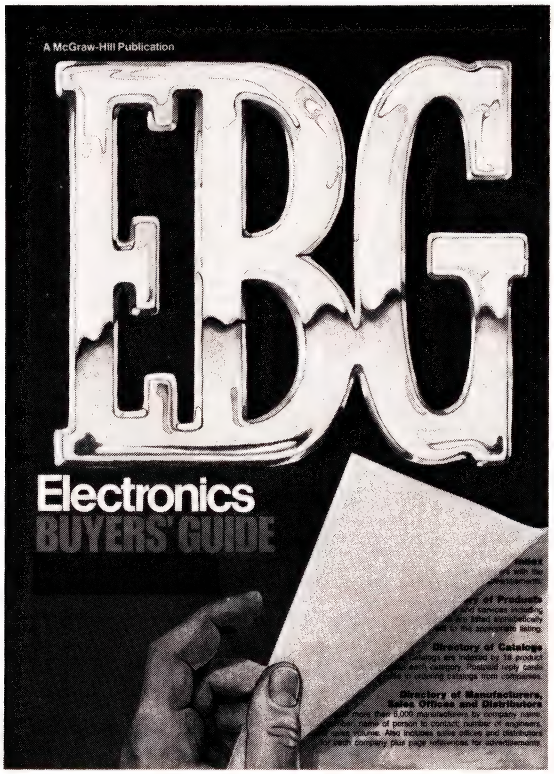
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CALAY AIMS TO USE CAD DATA TO BUILD AND LOAD BOARDS

Its CAM work station will take a giant step toward full automation in pc-board manufacturing; it converts CAD data for use in both board production and stuffing

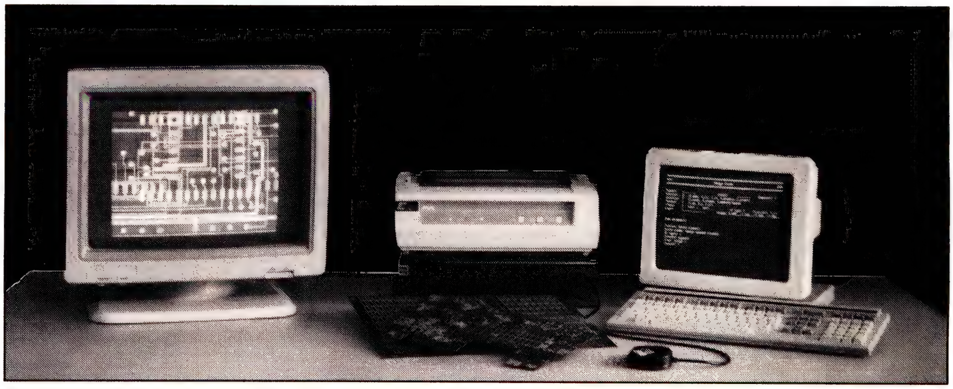
by Jonah McLeod

Work stations used in the manufacturing of printed-circuit boards trail their brethren in pc-board design: they are too new to have achieved the level of automation that computer-aided design work stations have. But now that's beginning to change, and one of the pioneers in bringing greater automation to computer-aided-manufacturing work stations is Calay Systems Inc. In February, the Irvine, Calif., company will roll out its ECAM (Electronic Computer-Aided Manufacturing) work station, a system that takes a giant step toward full automation. ECAM brings single-keystroke commands to the CAM world; it expands the repertoire of translators that convert CAD data for use in pc-board manufacturing, and it will include translators that convert CAD data for use in board stuffing.

ECAM marks Calay's first venture into CAM work stations. The five-year-old company made its mark in CAD stations for pc-board design and in fact is building on its CAD expertise to advance the state of the art in CAM automation. After running into financial straits, the company has regrouped (p. 64) and is introducing new CAD gear as well as ECAM. Other pc-board CAD companies also are moving into the market, and the CAM work station is fast becoming the catalyst for automating the entire board manufacturing process (p. 65).

ECAM (see fig. 1) is based on a Sun Microsystems Inc. work station: the 3/160, 3/260, or Sun 4. All run the standard Unix operating system. ECAM comes with at least 4 Mbytes of random-access memory and a 140-Mbyte Winchester disk drive. A hardware graphics accelerator and 19-in. color monitor with 1,152-by-900-pixel resolution are standard. Initially, the system will come in turnkey form at a price between $100,000 and $150,000.

Manufacturing engineers have long had access to work stations that offered some capability to convert pc-board CAD data for use in CAM work stations, but not to the extent that Calay does. What's more,



1. HELPING HAND. Calay's ECAM work station converts design data into data that can be used by most pc-board manufacturing equipment and by board-stuffing equipment and test gear.

Calay plans to introduce software that automatically acquires the needed design data from other manufacturers' CAD work stations. That software is due to be introduced in the second quarter of 1988.

Typically, the manufacturing engineer uses the CAD data to create a film phototool, the "mask" that replicates the printed-circuit pattern on a fiberglass panel, or form. Each panel will contain several of a single layer of the board.

To create the phototool—a process known as panelization—the manufacturing engineer must edit the artwork received from the CAD station. Editing is the first step in the manufacturing process (see fig. 2). He also must add to the artwork what are known as border features, such as test circuits. Adding border features usually is a time-consuming manual task, even in CAM work stations that use CAD data. The ECAM system introduces a set of powerful interactive graphics programs to the CAM world, so the engineer now can add each border feature through a simple, single command.

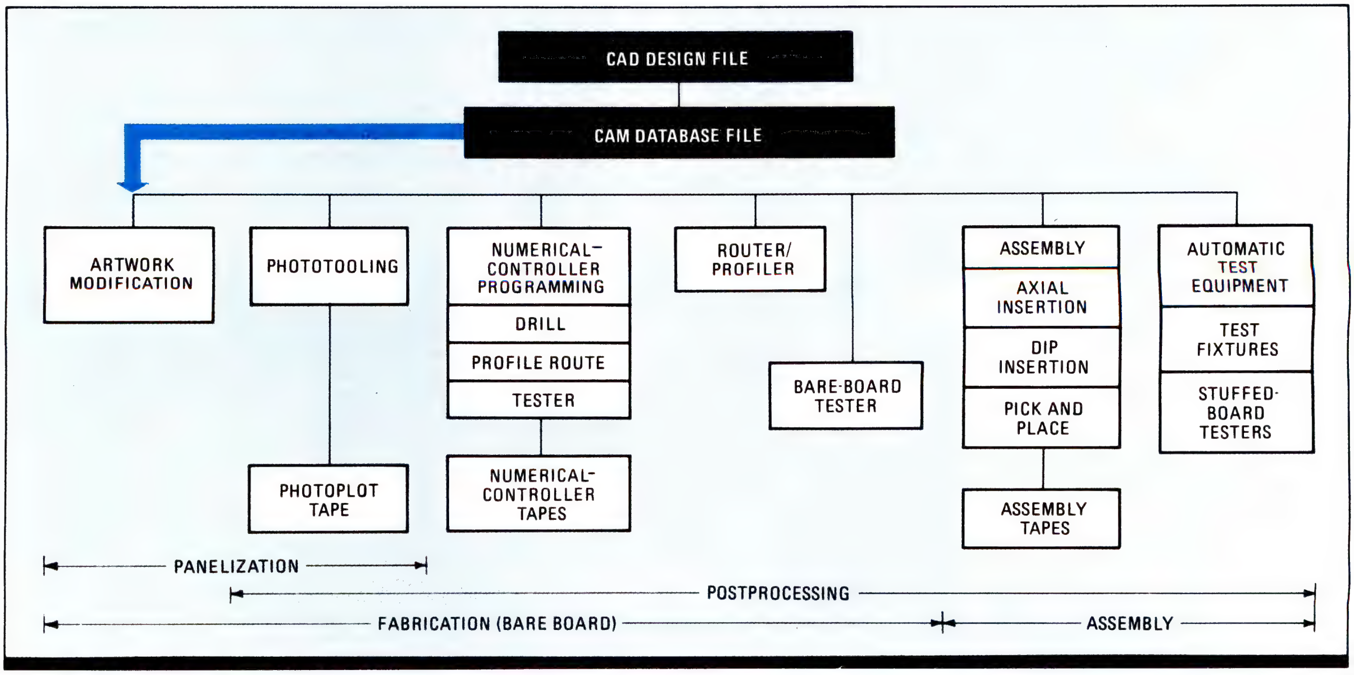
Another new editing feature borrowed from graphics processing is what Calay is calling a quick form tool. This allows an engineer to create any number of files, each containing a generic panel design that is missing only a board part number. When he or she wants to build a new mask with one of these generic panels, he simply specifies the part number of a board to be plotted and the name of a file containing the generic form. The system adds the board part number into the file containing the form and automatically builds a photoplot file.

To fabricate pc boards, the CAD data is converted into a photoplot, which a phototooling system can use to create the various board layers. Each layer is plated, the forms are laminated together, and a numerically controlled tool drills the holes for mounting components. Once the forms have been drilled, a router-profiler tool cuts the boards off the form. A bare-board tester ensures that there are no shorts or opens. All of these systems also can be driven by CAD data.

The software that converts the CAD data for CAM use is known as a postprocessor, and a different postprocessor is required for each manufacturing tool. No other CAM work-station maker provides as many postprocessors as Calay does, believes Steve Zizzi, ECAM product manager. "The work station already has over 31 translators and more are continually being added," he says.

Once the bare board has been made, it goes into assembly where the components are placed on the board. A variety of different equipment is found here: axial, radial, and DIP inserters; sequencer, verifier, and pick-and-place machines; and so on. Finally, automatic test equipment verifies the assembled printed-circuit board. At this point, no other CAM work station includes postprocessors that can drive all the assembly equipment. Calay plans to introduce such software in the second quarter of 1988; it need only port custom translators that it designed for some of its CAD work-station users. It will also produce files for the in-circuit and functional board testers.

Producing a board with the ECAM work station begins with the transfer of data from Calay's design work station. In the second quarter, Calay will provide data-base converters to allow ECAM to acquire the design data base from other manufacturer's work stations. For now, data from other work stations can be sent in the form of a Gerber data file (a format running on photo-



2. DESIGN AND BUILD. ECAM processes design data for phototools to build pc board layers and for drivers for other fabrication and assembly gear.

plotters from Gerber Scientific, Hartford, Conn., that has become a de facto standard). However, the format contains only the data needed to plot a board layout, so much design data is not present. The work station will also accept files in the National Bureau of Standards IGES (Initial Graphics Exchange Specification) format.

With ECAM's board-editing features, users work on screen to alter a board's physical characteristics—for example, the width of traces. Or, to speed the entry of text—part number, component nomenclature, and so on—the system provides a variable field that prompts the user to provide such information. As he enters these variables, the system automatically places the information at the appropriate location on the board design. On other systems, the engineer must create the text, determine where on the board it should go, and indicate the location to the system.

The ECAM system also removes unused pads. This capability is useful with edge connectors, for example, which have active areas only on the top and bottom layers. Yet every layer contains the connector in its artwork. "The engineer building the board wants to eliminate any unnecessary copper to free up space between active elements," says Zizzi. "By spreading elements apart using the freed space, there is less likelihood of shorts, and the board is more manufacturable."

It is easy for the ECAM work station to find unused pads since it can examine the design data to see which pads are connnected to an electrical signal, power, or ground. On many other CAM work stations, there is no such facility and the engineer ends up scraping the pads off the final phototool.

An ECAM user can enlarge or reduce all pads and traces at once or concentrate on individual pads and traces. To free up space on the board, he can squeeze tracks together or spread them apart. He can also add elements to the board. For example, he may want to add a "dead via," a hole drilled through the board with no connection. "Such elements are added to a board for mechanical reasons to improve cooling or to ease structural stress," says Zizzi.

An important part of editing is adding test circuits—called test coupons—at a number of dispersed locations around the printed-circuit patterns. "During manufacturing, pads and traces are added to test coupons on every layer," Zizzi explains. These coupons are removed from the final fabricated panel and tested to see if the laminations hold up under all extreme operating conditions, to determine how well the copper adheres to the fiberglass, to determine the thickness of the copper traces and pads, and to ensure all specifications. "In all, around 150 tests are performed on a test coupon," Zizzi says.

The manufacturing engineer also must add border features (see fig. 3) to the panel. These features, or patterns, are added around the perimeter of each printed-circuit layer on the form in order to facilitate plating and laminating. Adding the border features takes time on other CAM work stations because the systems lack ECAM's graphics-processing capability to automate the task.

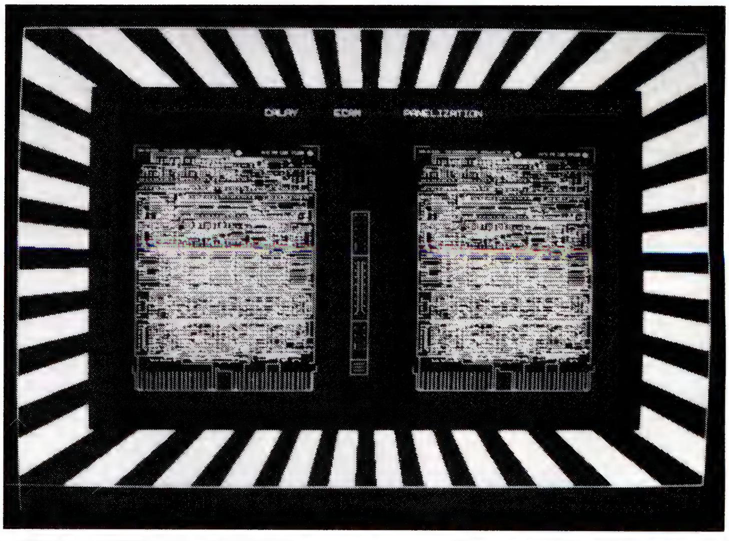
Two border features that must be added to every board layer are venting dots, small spacers between layers that allow the venting of any trapped air, and plating bars added around the layers of a board to facilitate more even distribution of the copper or silver-nickel plating material.

The panelization task, which creates a special file to drive the photoplotter, is only the first step with ECAM. The Calay work station also comes with postprocessors for other machines used in board manufacturing. One, the fabricator postprocessor, contains the drill-tape formatter and profile/router formatter. It also has a design-rule checker which ensures that the correct spacing width exists between traces, that pads are of the correct size, and so on. In the second release of ECAM tools, the fabricator postprocessor will produce files for bare-board testers.

ECAM can quickly translate design data; so if one n/c drill on a production line goes down, it takes only a few keystrokes to create a driver for another machine

The ECAM system provides "neutral" data-base conversion, that is, it can quickly convert design data into equipment-specific file formats. For example, a manufacturing engineer might create a file for an n/c drill machine that breaks down halfway through a run. With a few keystrokes, he can create a new file for an entirely different machine and resume the production run. On other systems, he would have had to manually change the file over to the new n/c machine. ☐

For more information, circle 480 on the reader service card.



3. FULL HOUSE. This ECAM-produced phototool builds two copies of one pc-board layer, separated by a test circuit and surrounded by plating bars.

THE RISE AND FALL AND RISE OF CALAY

Calay Systems Inc. got off to a fast start. Founded in 1982, it was the first company to sell computer-aided-design equipment with 100% automatic routing for work on printed-circuit boards. For three years, Calay dominated its slice of the CAD market.

But, inevitably, competitors caught up. And by the time they did, around 1985, Calay was starting to flounder. Deep-seated structural flaws made it virtually impossible for the company to fight off its new rivals. Quicker than it had risen, Calay plunged.

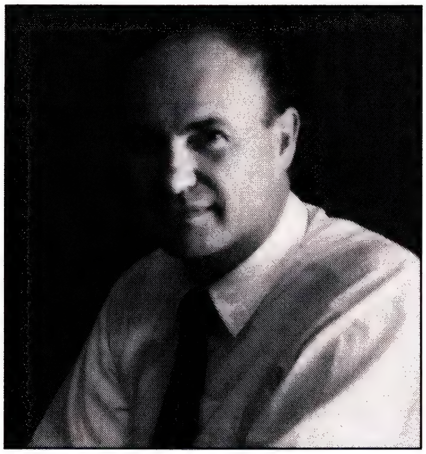
By August 1986, the company was in such serious trouble that it was forced to hire a noted corporate "doctor," Peter J. Shaw, as president. Shaw says that when he took over Calay's condition was simple but critical: acute "financial hemorrhaging."

Now, things are looking up again. In one year, Shaw stanched the bleeding. More important, he bandaged the wounds. New management was brought in and the former president and the vice presidents of sales, finance, and operations were ushered out. New staff was hired. Tighter controls were imposed on operations. Tangled lines of authority were straightened and simplified, an effort that culminated in a change of ownership, with AGIV, a $2 billion holding company based in Frankfurt, West Germany, taking over.

With that accomplished, Shaw has stepped aside as a day-to-day manager. Peter K. Maeussnest, a former consultant who had tried to acquire Calay himself, now serves as president and chief executive. Shaw, now back at the Shaw Group, his consulting firm in Orange County, Calif., still acts as a consultant to Calay. Both men say Calay is making the right moves toward regaining its front-runner position.

As an example, they point to the new ECAM work station (see p. 61), which links CAD equipment closely with the factory floor by presenting product design specifications in a format useful to manufacturing engineers. It not only ties into Calay's own CAD gear, but will also offer an open architecture that can interface with equipment from other vendors.

The CAD equipment, Calay's original product line, is being upgraded, too. The company is preparing its latest generation, the V05 line of CAD work stations and software. In the process, it is upgrading the hardware from 16 to 32 bits, a move Maeussnest likens to installing a new engine in an automobile.



MAEUSSNEST: Calay's new CEO has taken over the job of rebuilding the company.

ECAM and the new VO5 line represent what has always been Calay's strength: "a fundamental core of technology to build on," in Shaw's words. The problems lay with the company that was trying to do the building—its operations were widely dispersed and corporate authority was fragmented.

Calay is actually four companies: Calay Systems GmbH, based in Frankfurt; Calay Systems Inc., based in Irvine, Calif.; Calay Systems Ltd., based in Tokyo; and Calay Systems Asia PTE, based in Singapore.

In theory, the German company developed the technology for Calay products. Both the German and the U. S. companies built the hardware, which the U. S. company marketed. The U. S company then transferred the hardware to the Japanese and Singapore companies. They customized the equipment for the local markets.

In practice, those operating units grew so autonomous that effective teamwork evaporated. The Asian companies never meshed properly with their American and German counterparts. The U. S. company went beyond its role as manufacturer and marketer to strike out on its own in engineering.

To make matters worse, ownership was split among several shareholders in both Europe and the U. S., including Summit Ventures Inc. of Boston and the German technologists who had originally started the company. None was the undisputed leader of the company. "They could not resolve who ran it," Shaw says.

The problems went further than simple confusion. The owners had sharply divergent views on what the company ought to be doing. "Technological entrepreneurs in Europe and venture capitalists in the U. S. don't usually see eye to eye," Shaw remarks. Generally, the entrepreneurs took a long-term view; the venture capitalists wanted short-term payoffs.

Shaw's solution went to the heart of the problem. He found a single owner to replace the numerous shareholders. In July, AGIV bought out all parties. This move, along with enhanced financial resources, paved the way for the arrival of Maeussnest, who is now shuttling between Germany, the U. S., and the Far East.

Calay's rebuilding is far from over. While the company was struggling, its competitors were solidifying their market position. Some of them, such as Cadnetix Corp. and ComputerVision, are many times the size of Calay, which now has about $25 million in sales annually. But Shaw, for one, is not discouraged. "Smaller size can be an advantage in moving faster," he says. Calay needs to move fast—it has a lot of lost ground to recover. *–Larry Waller*

NOW, WILL CAM FINALLY CATCH ON?

Automation of pc-board production gets closer as CAM stations link up with CAD stations and phototools; but designers slow process by objecting to CAD data going to factory floor

by Jonah McLeod

Producing printed-circuit boards has always been a tedious, time-consuming task. The advent of laser phototools in the late 1970s, followed by computer-aided-design work stations, began to change all that, and since then the goal has been to automate as much of the job as possible, if not all of it. That goal—full automation—is getting much closer as new work stations for computer-aided manufacturing are beginning to hook up with CAD stations on the front end and laser phototools on the back end. Within a short period, manufacturing pc boards may be a totally hands-off enterprise.

Now valued at $100 million, the CAM work station market should grow faster than 40% over the next five years. Whereas first-generation CAM work stations concentrated on improving the panelization task, which involves only the laser photoplotter, the current crop is providing data to run ever more production equipment. And the latest CAM work stations are acquiring design data from various CAD data bases despite strong objections from designers who are reluctant to give production engineers the ability to change board designs.

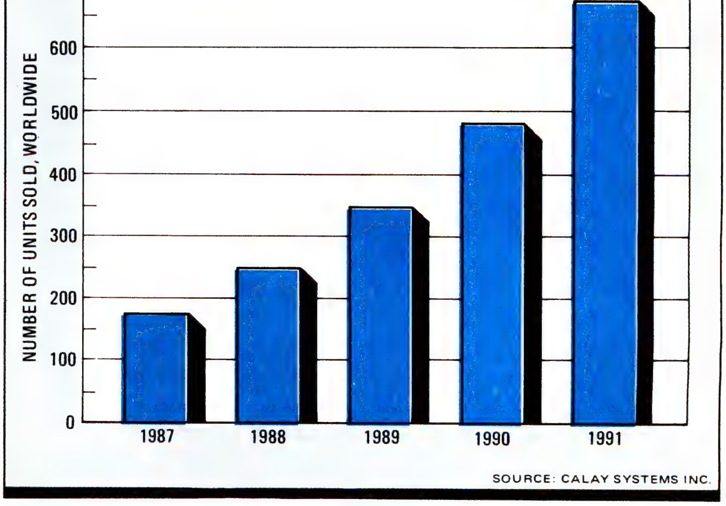
The symbiosis of work station and photoplotter is the catalyst for automating the entire manufacturing process for printed-circuit boards. John Salzer, president of Salzer Technology Enterprises Inc. a market research firm based in Santa Monica, Calif., estimates that the worldwide installed base of laser photoplotters alone will triple, to almost 500 units, by 1991. "One source of sales for laser photoplotters is the installed base of 2,500 conventional photoplotters," says Salzer. These are typically in a board design lab where a designer produces a single-copy film of each board layer, which he provides to the manufacturer of the board. Moreover, each photoplotter sale should generate a demand for more than one work station. A laser photoplotter can cost as much as $500,000, but it can serve more than one work station, which typically costs less than $100,000. So it makes economic sense for a photoplotter purchaser to buy several work stations to keep the plotter busy.

Jeffrey Rittichier, product marketing manager for electronic systems at Gerber Scientific Inc. of South Windsor, Conn., estimates that there are between 600 and 700 sites worldwide that could use laser phototools, which represents a total available market of around $300 million. In addition, Steven Zizzi, ECAM product manager at Calay Systems Inc., Irvine, Calif., says that by 1991, sales of CAM work stations could hit 675 units, worldwide (see graph).

Conventional plotters make sense in the design lab because the volume of film (the photoplotter "masks") is relatively low. But "laser photoplotters make much more economic sense on the manufacturing side of the house where many more board designs [pieces of film] are handled," Zizzi explains. Potential customers for laser photoplotters and CAM work stations divide into two categories: captive and merchant pc-board production shops. "Noncaptive shops produce 57% of the pc-board dollar volume, but they represent 72% of all the shops making boards," Zizzi asserts. "The average size of a noncaptive manufacturer is about $3 million in annual sales, compared with about $6 million for captive board makers."

In the U. S., there are 930 board manufactur-

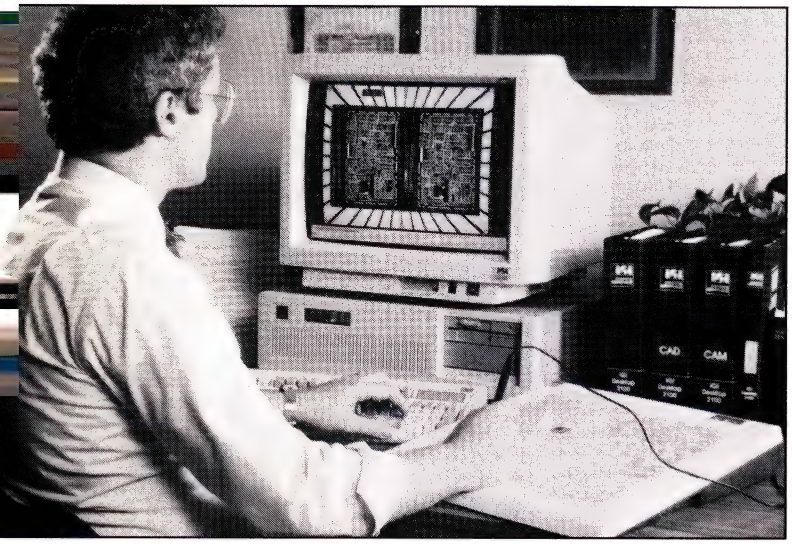
CAM WORK STATIONS WILL BLOSSOM



SOURCE: CALAY SYSTEMS INC.

ers with under $2 million in annual sales, and only 11 makers with over $50 million in sales. Eight laser phototool manufacturers are competing in this market and are providing CAM work stations. In addition, CAM work stations that will provide data to most commercially available photoplotters are coming from makers of CAD work stations for pc boards: Calay Systems Inc. of Irvine, Calif. (see p. 61), Cadnetix Corp. of Boulder, Colo., and Royal Digital Systems Inc. of Palo Alto, Calif.

Until the advent of laser photoplotters, a designer worked with CAD systems and conventional photoplotters to create a positive film of every layer of a pc board. He then provided these to a production engineer. "Each layer can take an hour with a conventional photoplotter," says Jerry Harvel, executive vice president of Royal Digital Systems. Using a step-and-repeat camera, the production engineer then manually creates a larger piece of film—or phototool—containing repeated images of one layer of the pc board. This process is called panelization; and it is required because manufacturing makes more than one pc board at a time.



1. TIMESAVER. Infinite Graphics' IGI-2000 allows operators to generate tooling artwork at the rate of 10 layers an hour.

A fiberglass panel that can hold four copies of a board layer requires a phototool with four images—and a critical concern in panelization is that the four images of the first layer fall precisely in the same place as the four images of all other layers. So the phototool must be precise. With some high-density boards, the production engineer must compensate even for expansion or contraction of the film. Besides taking the time required to replicate the layer's image, the production engineer must strip in other features, such as test circuits and any text that must go on the board. The process is akin to artwork preparation in a printing process.

The laser photoplotter market got off the ground in 1983 when Eocom, then a division of American Hoechst Corp. in Somerville, N. J., sold the world's first laser photoplotter. In 1984, Gerber Scientific bought Eocom and built its own CAM work station that uses CAD data to drive the plotter. The company also wrote its own panelization software, which ran on an IBM Personal Computer AT or compatible system.

At the same time, Infinite Graphics Inc., a Minneapolis service house that produces boards from its customers' design data, developed panelization software for its Gerber photoplotter. The software, which also runs on an IBM PC/AT, was subsequently offered as a separate product, the IGI 2100 Panelization System (see fig. 1). "It was the first panelization software package," says Clifford Stritch, president and chief executive officer of Infinite Graphics. "With panelization software on a work station, the production engineer could create in eight minutes an entire panel for every layer on the board and then plot the entire panel."

In 1986, McDonald Deitweiler Associates of Richmond, B. C., Canada, which had brought out its own laser photoplotter to compete with Gerber, purchased the IGI 2100 software and ported it to the Data General minicomputer family. "MDA is credited with developing the market for photoplotters and automated panelization," says Stritch.

But panelization software was only the starting point for fuller automation in pc-board manufacturing, says Stritch. "CAM work stations from photoplotter manufacturers have concentrated on improving panelization for the production engineer," he says. "But we believed from the beginning that panelization was only part of the solution. What was really needed was software that could take the entire CAD data base and build the input files needed by every piece of manufacturing equipment in the board production process."

New-generation CAM work stations from traditional CAD work-station suppliers have begun to do just that by providing translation software that creates data files for specific production equipment. Three examples are Calay's ECAM system, the Manufacturing Work Station (see fig. 2) that Cadnetix introduced in July, and Royal Digital's Panelization Station, introduced this month. These systems, and the latest version of the IGI 2100 Panelization System, all provide the output files needed to drive numerically controlled tools, routers, and bare-board testers.

On these work stations, after the panelization process is through, a production engineer extracts the data needed for, say, n/c drill equipment. He then specifies the sizes and types of holes to be drilled, and the format required by the drill. "The translator program is sophisticated enough to sort through the graphics data and arrange the instructions to the drill machine to optimize operation," says Robert Anastasi, director of CAD/CAM marketing for Cadnetix. For example, the program will instruct the n/c tool to drill adjacent holes rather than have the tool move back and forth across the board surface, drilling holes randomly.

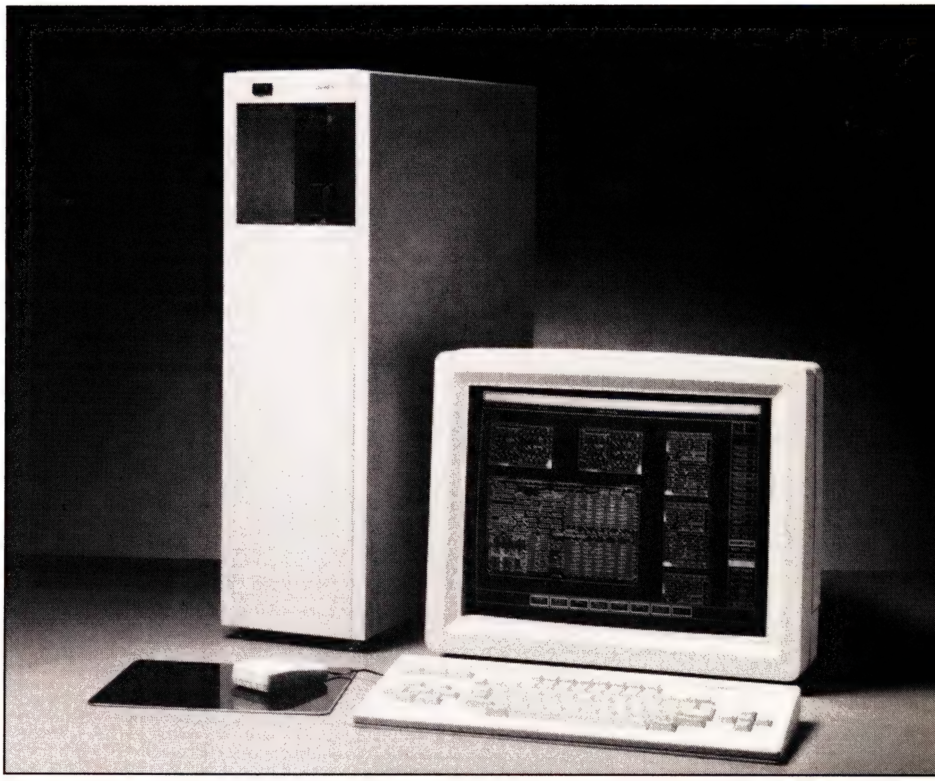
CAM work-station suppliers are working to provide a more complete set of translators. Calay, for example, boasts 31 different translators for various production equipment. At Cadnetix, "we recognize that there is a lot of custom equipment in the manufacturing area," notes Jim LeBrun, product marketing manager. "So we have added an English-like data query language, which allows a foreign piece of equipment to access every piece of data in the Cadnetix work station's data base."

Harvel at Royal Digital Systems agrees that providing open access to CAM data is essential if the production floor is to achieve true computer-integrated manufacturing. "Our work-station data base is available and can be easily configured for any existing or new piece of production equipment," he claims. And computers, as well as automated production equipment, can access the CAM work-station data base. LeBrun cites the instance of a computer wanting information on the manufacturing process. "The Cadnetix system collects data on the number of drill holes in a board and the distribution of the hole sizes," he explains. "In a CIM environment, the central computer could digest that information to determine when to change drill bits in the n/c drill equipment."

The last obstacles to full automation—lack of standards for moving CAD data into CAM work stations—are being hurdled. "Data-base translators alone are not enough," says Harvel. "The problem with moving CAD data into the CAM environment is that designers are resisting releasing the CAD data base to manufacturing," Calay's Zizzi explains. "They do not want manufacturing [engineers] changing board layouts." Designers have relinquished the Gerber file, the familiar format that drives a photoplotter, because it contains only graphical information on locations of pads and routes for every layer. "There are over a couple hundred Gerber formats, but the one running on the older Gerber Vector Plotters is the one cited when everyone refers to Gerber file format today," says Gerber's Rittichier. An Electronic Industry Association RS274D specification standardizes this file format.

IGI's Stritch says that, over the long term, companies building their own pc boards will eventually provide design data to manufacturing in order to remain competitive. "One of the most compelling reasons for doing so is to improve quality and reduce cost," he explains. He cites the example of automatic optical inspection, which compares a known-good board layer with layers that have just been fabricated. "If the standard is bad, it can easily cost a manufacturer $50,000 before the error is caught in final board test," he says. The mistake could be avoided easily by comparing the layers that have just been manufactured against an electronic image of the layer, derived from the CAD data base.

Such costly errors are the reason that companies building boards on government contract and major captive-board manufacturers are moving CAD data to manufacturing. With government contracts, the data is likely to arrive in IPC-350 format, a Department of Defense standard. Captive-board makers likely will provide data in the Calma GDS II Streams format or in a CAD-system-specific format—such as the Cadnetix or Calay data-base format.



2. FABRICATOR. The CDX-6000 gives fabrication gear CAD data it can use.

In the future, once the Electronic Design Interchange Format (EDIF) becomes a standard, it will be universal. "Until that time, we will be developing software tools that will allow production engineers to reverse-engineer CAD data from the Gerber file information," Stritch declares. Such products will be forthcoming in the first part of next year. "Another alternative to having the complete CAD data base is to combine the Gerber data file with a netlist of the design," LeBrun of Cadnetix offers. Data in the netlist is essential if the CAM work station is to provide a file to a board-stuffing machine. ☐

EDGE FINDS A WAY TO RUN TWO OPERATING SYSTEMS SIDE BY SIDE

Its Symetrix architecture lets Unix and Pick run as peers with no degradation

by Tom Manuel

A new software architecture that lets two or more operating systems run on the same computer with no degradation in the performance of either is now at hand. Called Symetrix, the package initially will support the Unix and Pick operating systems. But its maker—the Toltec Systems Division of Edge Computer Corp.—says that Symetrix will be able to handle other operating systems as well. It was designed for Edge computers and other machines based on the Motorola 68000 microprocessor family. It could, however, be adapted for other processor instruction sets.

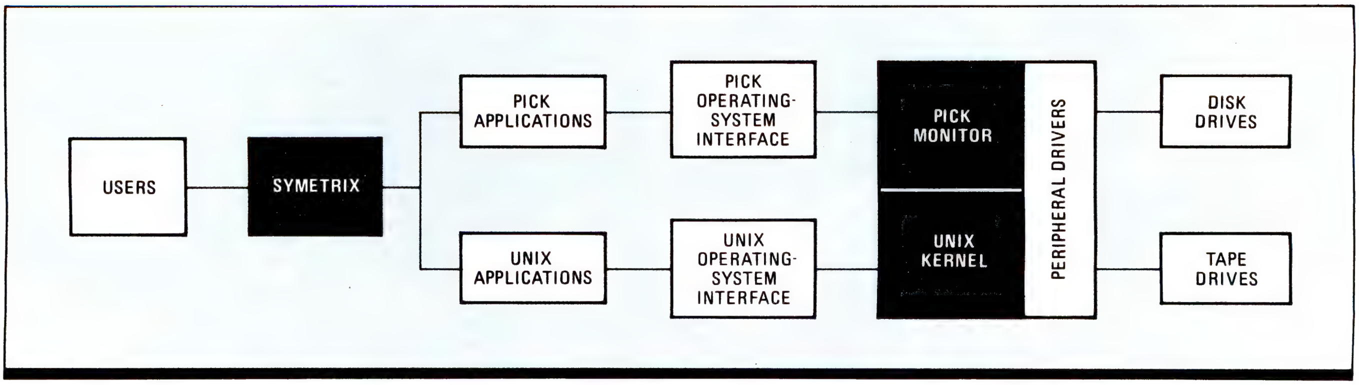
Symetrix appears just as computer users are grasping for ways to get added value from their machines by running two or more operating systems concurrently. The more operating systems a machine can handle, the more applications programs will be available to it. But the hitch has been reduced functioning: typically, performance is sacrificed because one operating system runs as the native on the machine and supervises the others. The Symetrix multiconcurrent operating-software architecture overcomes this disadvantage by allowing the operating systems to run as peers on the same computer, each having control of the machine and each running at full native performance.

Symetrix 1.0, available now, combines full-function versions of AT&T Co.'s Unix System V, release 2, and the Pick Systems Pick Open Architecture, version 1.2. Both are popular operating systems, each with many applications programs. Symetrix Version 2.0, with many more features, will be available in the first quarter of 1988. And while Toltec is keeping mum about releases beyond Version 2.0, the Symetrix architecture makes possible many other combinations, such as adding MS-DOS.

Through the Scottsdale, Ariz., division, Edge will market to end users and value-added resellers complete systems combining Symetrix software on the Edge computers for which it was created. The company will also adapt Symetrix for other machines that use the Motorola 68000 microprocessor instruction set. "Technically, there are no inhibitions to porting Symetrix to other 68000-based machines," says Al Dei Maggi, Edge's vice president of marketing. "We will make [Symetrix] available through licensing at a reasonable cost; and we will promote it as a standard for multiconcurrent operating systems." Licensing fees have not yet been set.

Getting two or more operating systems to run as peers, extracting equal efficiency from a single machine, was the prime challenge for the Toltec team. A second goal was a common file and input/output service for the two operating systems. Once these aims were achieved, the team found that the door was open to allowing programs running under the different operating systems to share data and use each other's services and features. File sharing, memory sharing, and execution of processes across contexts are among the ways this can occur. To top it all off, the software engineers developed a common menu-oriented user-interface shell. This feature lets applications developers give end users a simple way of running applications and isolating them from the operating systems.

The Toltec team had decided at the outset of the Symetrix project a year ago that it was crucial for both operating systems to get equal



1. NO COMPROMISE. In Symetrix, the Pick monitor and the Unix kernel sit atop the commonly shared I/O service layer.

dibs on the hardware resources of the machine. "The first and foremost design goal was to have Pick and Unix run as co-residents in the supervisor space of the 68000 memory," says Gary Epple, Edge's director of software engineeering. "And while it is running, either operating system would have [at its disposal] the full native performance of the machine."

In the overall structure of Symetrix (see fig. 1), the Unix kernel and the Pick monitor sit atop the commonly shared I/O service layer, which contains peripherals drivers. At the top level, users have access to both Unix and Pick applications through the menu-oriented shell, the common user interface. The applications can have standard interfaces to their respective operating systems and need not be altered to run under Symetrix.

The ability to execute two operating systems side by side comes from a software module called the Hypervisor. As a Symetrix system comes up, the Hypervisor first brings Unix up in the supervisor memory space. Then Unix carves out a part of the supervisor space for the Pick operating system and then loads it.

Since the operating systems co-reside, the Hypervisor performs the complete context switching required for both to share the central processing unit. To switch contexts, the Hypervisor saves the contents of all registers and loads up the values for the other operating-system context. The context-switch code is only about 100 instructions—it takes about 10 µs to execute on the Edge 1000.

The shortest time that the Hypervisor can let one of the operating systems run is 4 ms. Two things determine when a switch is made. First, system administrators can set the number of 4-ms ticks for each operating system, depending on the mix of jobs and users. Secondly, a continous dynamic balancing takes place automatically. When either operating system goes idle—all jobs are finished before the allotted time slice is over—Hypervisor switches to the other operating system. That way, no time is lost in running the two operating systems concurrently. The computer operates just as it would under one system.

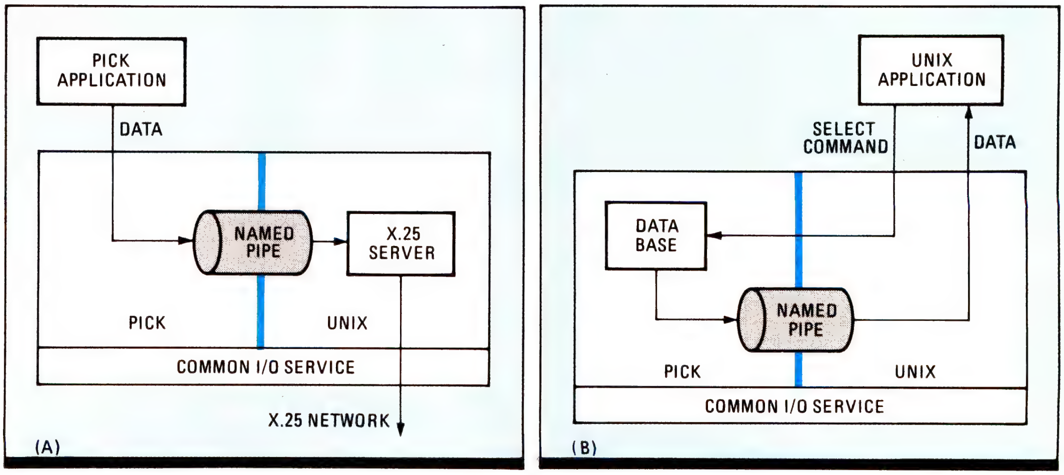
The Hypervisor provides no direct communication between operating systems. But since the systems and the applications share the same machine—CPU, main memory, file system, and I/O subsystems—it makes sense for programs to also share data, and for processes in one operating environment to be able to communicate with processes in the other. The engineers used a basic file-sharing mechanism in version 1.0 of Symetrix and are creating much tighter coupling and interprocess communication facilities in version 2.0. This tool gives each operating system a set of jump tables, located on its side of the supervisor space, to use in requesting file and I/O services. In version 1.0, the basic level of file sharing uses these jump tables plus special processes running under each operating system.

For example, when a Pick program wants to access data from a Unix file, it passes a Unix Open command to a so-called Unix daemon, a process waiting on the Unix side for Pick requests. The daemon then performs the Unix file access. Similarily, a process running on the Pick side and called a Pick phantom can access Pick functions when it gets a request from Unix.

The common I/O service layer is implemented with Unix device drivers, so the Pick side transparently gets the benefits of the varied features of the Unix drivers. Standard Pick I/O calls are issued by the programs, but the real Pick I/O drivers have been replaced by virtual device drivers that intercept the calls, reinterpret them as Unix calls, and send them to the I/O service.

Toltec is also incorporating in the common I/O service layer some Unix transaction-processing extensions that it purchased from the now defunct EnMasse Computer Corp. Among them are a fault-tolerant file system using mirrored disks, enhanced terminal handling for large numbers of transaction-processing users, and a full-function transaction-management system containing transaction logging. The mirrored-disk feature automatically records data on two different disk drives to assure data integrity in the event of disk crashes. The intelligent-terminal-handling software improves response time and productivity. In the event of a system fault, transaction logging reconstructs and restores partial transactions.

These features are being incorporated gradu-



2. HANDY PIPES. Symetrix uses named pipes (a Unix interprocess communications feature) to link Pick and Unix. A Pick application uses a Unix service (a) and a Unix application can access a Pick data base (b).

ally, but at least one of them—the fault-tolerant, mirrored-disk file system—will be available in Symetrix version 1.0. Intelligent terminal handling will be included in version 2.0, while transaction logging will be added later next year—late in the second quarter or early in the third.

Perhaps the single most important feature being added to version 2.0 is interprocess communication, which provides tighter coupling between the operating systems. This is a system to provide the facilities for intercontext execution as well as sophisticated file sharing between Pick and Unix processes. The system achieves this kind of communication in three ways.

First, it uses named pipes, a Unix interprocess communications feature that is a way of connecting two processes; it becomes available to Pick as well. By transferring data through named pipes, the two systems can share any type of file or I/O and communications services. An example of such intercontext execution might be a Pick application transferring data to an X.25 packet-switched network server process on the Unix side and subsequently transferring data over an X.25 virtual circuit (see fig. 2a). Likewise, a Unix application might run a Select operation on a data base using Pick's sophisticated relational data-base management system (see Fig. 2b).

The second means of achieving interprocess communications is through shared memory: Pick applications will get an interface to Unix's shared-memory facilities. This means, for example, that the run-time statistics being gathered by each operating system could be accessed by a single analysis program.

Finally, the third interprocess communications facility is the Unix System V semaphore, which is a software mechanism for coordinating cooperative processes.

Thanks to another aspect of Symetrix, end users can enjoy this dual access while never having to worry about it. That's because of the shell, a common menu-oriented user interface hiding both operating systems from the end users. Applications programs can be installed under the shell and the menu can be customized by a dealer to create application-specific interfaces to his products. Some of the programs in an application may be running under Unix and the others under Pick—the user need not know or care which.

In all, Symetrix will be an excellent software environment to team up with the forthcoming Edge 2000 multiprocessor system [*Electronics*, Sept. 3, 1987, p. 66] driving high-availability, high-volume, transaction-processing applications. This powerful combination will allow Edge Computer to compete in a new marketplace. ☐

For more information, circle 481 on the reader service card.

HOW TWO ALIEN SOFTWARE WORLDS LEARNED TO COEXIST

Before Toltec could bring the Unix and Pick operating systems together via Symetrix, it first had to bring two teams together from the very different software worlds those systems had spawned. And that was no simple matter, say team leader Gary Epple and Toltec founder Al Dei Maggi.

At the project's start, the two groups were just not communicating. "It was interesting," says Epple, director of software engineering at Edge Computer, of which Toltec is a division. "It was an issue of ownership and 'not invented here.'" Each side had its own "best" way of doing things. Pick people work in assembly language, for example, while Unix people write structured code in the C language. And their debugging tools are utterly different.

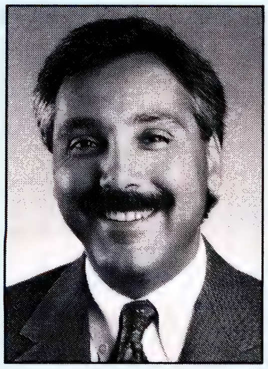
Epple's response was to throw the Unix and Pick people together in the same room in what he calls "joint investigation sessions." Each side would present its approach to solving a problem, such as disk optimization. Then they would together hammer out the best way to handle it for Symetrix. After a few such sessions, things got better. "Now they talk and want to learn about both sides. They work together extremely well," says Epple.

The dueling and sparring began in the spring, after Dei Maggi—then president of the startup Toltec—went looking for a partner with a good hardware platform and expertise in Unix to share his aim: bringing sophisticated new features to the Pick environment, especially the communications capabilities offered by Unix. The partner was Edge, which in March bought a 51% interest in Toltec and this month announced it would buy the rest. Dei Maggi is now Edge's vice president of marketing.

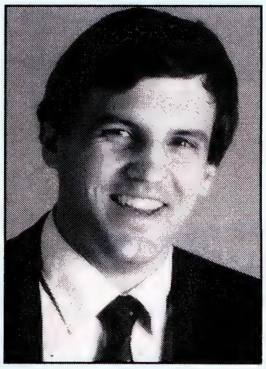
Dei Maggi had begun Toltec a year ago, created the product specification for Symetrix, and recruited a small cadre of Pick software experts. His technical strengths are in understanding transaction processing, and the integration and communications issues that it involves. He found in Edge "a lot of Unix experience" and a commitment to "staffing the Unix side of the engineering project." Among the company's resources was Epple, who had worked with Unix for many years at Honeywell, A. B. Dick, and Wang before coming to Edge some 3½ years ago. In March he took on management of the eight-member Symetrix team.

"My whole background is in porting system software," he says, and in tuning systems for high performance, a big part of the Symetrix effort. But first came the challenge of getting the Unix and Pick sides of his team working together.

A metaphor for that process can be found in the project name. When work began, the team was calling the system they were creating Pick-and-Unix, exemplifying its schizoid nature. "It helped a lot," says Dei Maggi, "when we started calling it Symetrix: a single entity with two sides to it." *–Jeremy Young*



AL DEI MAGGI



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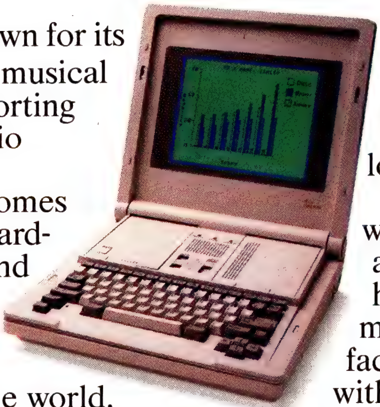

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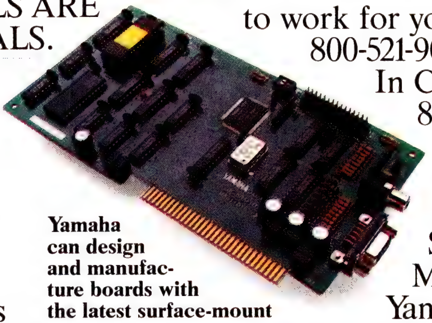

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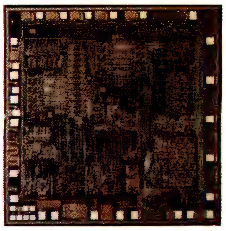

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DATACUBE World Review

VOL. 0 ISSUE 4

FIRST QUALITY IMAGE PROCESSORS FOR NON-RS-170 DEVICES.

INSIDE:

- **Good News For IBM PC/AT Users**
- **Datacube's Sales Are Zooming**
- **MaxWare Makes Complex Image Processing Easy**
- **Frame Stores For All Popular Buses**

DSP Module Performs Up To 100 Times Faster

EUCLID, Datacube's super-fast DSP processor module can perform mathematical operations at up to 8 million instructions per second. Based on Analog Devices' ADSP-2100 digital processing chip, EUCLID represents a significant milestone in DSP microprocessor architecture. By augmenting the on-chip parallelism of the ADSP-2100 with additional on-card hardware, EUCLID is able to do sequential processing tasks in parallel. The result is a single board that performs up to 100 times faster than a 16MHz MC68000.

EUCLID fills the gap in processing system design between fast, specialized hardware-intensive solutions and slower, more flexible software-based solutions. EUCLID's on-board hardware includes a writable program store, dual-ported data storage, a memory-mapping unit (MMU) for extended ADSP-2100 address space, a master/slave VMEbus interface, and a MAXbus region-of-interest (ROI) interface. The module also includes an ANSI standard "C" compiler with in-line assembly facility and a library of ADSP-2100 optimized image processing and numerical routines, callable from "C" or assembly languages.

Datacube's MAX-SCAN is a programmable, asynchronous input module which digitizes images with resolutions and frame rates which do not match the RS-170 standard.

This real breakthrough brings low cost, real-time image processing to many industrial and scientific systems using video sensing devices such as line scan and area scan sensors.

In fact, MAX-SCAN supports most video formats. It accommodates both slow frame rates from sensors like scanning electron microscopes and fast frame rates from devices like radar scanners. Its many features include programmable line length from 1 to 4096 pixels per line ... plus a programmable threshold Horizontal Run Length Encoder that stores the positions of grey scale transitions.

With MAX-SCAN's wide range of programmability it can handle the full range of image resolutions from as low as 1 x 1 to as high as 4096 x 4096 pixels, and frame rates from tens of seconds up to the 1000 frames per second range.

MAXbus Recognized As Digital Video Interconnect Standard

Experts give Datacube's MAXbus much of the credit for the unprecedented success of the MaxVideo family of image processors. Its open architecture and its noise immune ECL design have made the MAXbus digital video interconnect the standard for the entire industry.

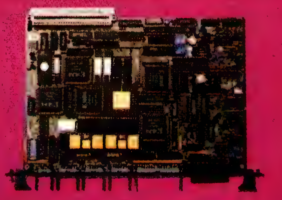
MAXbus gives the user more ways to define and control the data pathways between the individual boards in an image processing system. Now, signal processing architectures can be changed in software because MAXbus data paths are more programmable then ever before. And MaxVideo systems can be expanded whenever additional processing power is needed because MAXbus interconnect cables are so easily reconfigured.

MAXbus has none of the bandwidth or pipeline configuration restrictions inherent in most other signal processing systems. Its flexibility and expandability have been key in its acceptance as a standard.

Sales/Service Organization Expands

Datacube's commitment to provide top notch customer service is clearly evident both in the US and overseas. The company continues to upgrade its rep and distributor network in number and in the degree of management and training support provided. A toll free 1-800 customer assistance hot line gives Datacube customers the support they require.

At last count, Datacube's field organization exceeded 350 people working from over 60 offices. Their goal is to provide in-depth technical assistance wherever it is needed.



ROI-STORE, a region-of-interest framestore, and MAX-SCAN, a digitizer for asynchronous sensors, are two of the newest modules in the MaxVideo family of real time image processors.

Widely recognized as the standard for the industry, MaxVideo now offers 19 unique modules. Each one supports several types of image processing operations. Customers pick and choose only the modules required to implement their particular applications. Processing power can always be increased by adding another module.

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HERE COMES HIGH-POWERED UNIX FOR MULTIPLE CPUs

BBN Advanced Computers is building a multiprocessing Unix around Carnegie Mellon's Mach operating-system kernel—and Butterfly Plus hardware to run it

by Lawrence Curran

BBN Advanced Computers Inc. is taking the wraps off a new operating system that promises to make waves in the world of parallel computing: a high-performance, multiprocessor version of AT&T Co.'s Unix. The Cambridge, Mass., parallel-computer pioneer has also unveiled a massively parallel new hardware base, the Butterfly Plus, along with two stand-alone computers built around it.

The new operating system is Mach 1000, the first large-scale, parallel-processing, commercial system to evolve from Carnegie Mellon University's Mach multiprocessor operating-system kernel, which in turn is based on Berkeley Unix 4.3 bsd. It will be offered along with the company's proprietary Chrysalis operating system.

Mach was meant to be a true multiprocessor implementation of Unix. BBN has modified it in its Mach 1000 operating system to offer extensive support for networking protocols, including the TCP/IP standard, and make it easier to implement flexible virtual memory. For example, it allows two processors to share the same memory address space while protecting against overwriting, and it also supports sparse address space more easily than Chrysalis does.

The new hardware, meanwhile, boosts the performance of each node in BBN's current-generation Butterfly architecture from 1 million instructions per second to 2.5 mips. All this power is available at half the price of the hardware it replaces: $5,000 per mips. What's more, Butterfly Plus increases overall system performance from 250 to 600 mips for the maximum configuration of 256 processors, and also offers 1 gigabyte of shared memory.

The Butterfly Plus is the heart of a new general-purpose computer, the Butterfly GP1000, which will be available next March. The machine is intended for applications developers seeking higher performance in such tasks as production scheduling, circuit simulation, molecular modeling, and expert systems. Later next year, BBN will unveil the Butterfly RT1000, which is aimed at real-time simulation, scheduling, image understanding, signal-processing, and telemetry applications. Though both machines will share the Butterfly Plus architecture, only the GP1000 will offer the Mach 1000 operating system. The RT1000 will be equipped instead with both a pSOS real-time operating system and a VMEbus now under development. The computer will be beta tested the second half of next year.

For BBN, the two developments represent the first expansion beyond the Chrysalis operating system and the first fruits of a $32 million fi-

1. A MONARCH. The king of the Butterfly computer product line is the new GP1000 with up to 256 of the new double-speed processors.

nancing arrangement and limited partnership with Paine Webber Development Corp. announced just last spring. The financing came less than a year after BBN was spun off in July 1986 as a subsidiary of Bolt Beranek and Newman Inc., the pioneer network and communications company. Its charter is to continue to develop parallel-processing computers based on the Butterfly processor and switch technologies.

While the hardware enhancements embodied in the Butterfly Plus architecture are important to the GP1000's improved performance, the machine's ability to offer the Mach 1000 operating system is crucial. BBN engineers have enhanced Carnegie Mellon's Mach multiprocessing kernel to enable it to make the best use of the interprocessor synchronization mechanisms provided in the Butterfly architecture.

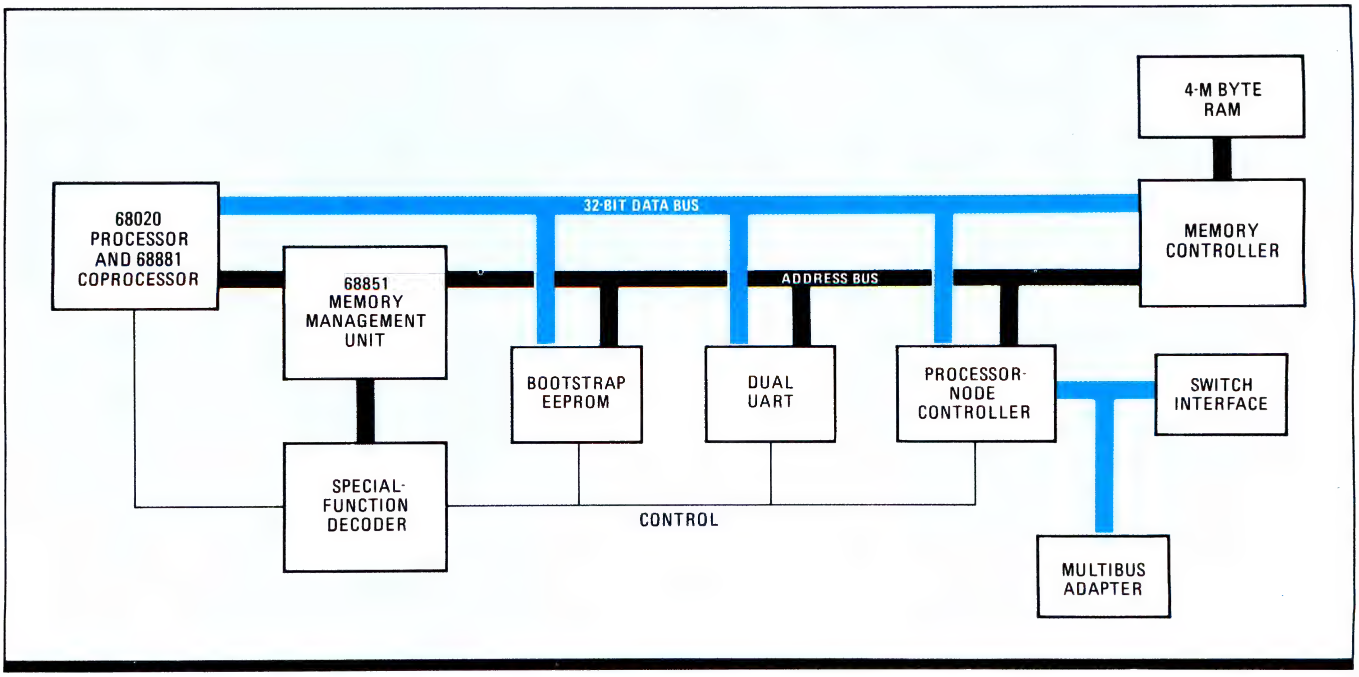
Among these mechanisms, now supported by Mach 1000, are atomic operations. An atomic operation, such as an atomic read, is an operation that can't be interrupted. This protects the integrity of one process from another. For example, a read involving a reference through the switch to a remote memory location can't be interrupted. Atomicadd, atomicor, and atomicand are atomic operations that allow programmers to guard critical regions and maintain data consistency for memory shared among processors.

And while Unix is a time-shared system, Mach 1000 allows users to dedicate certain processors to higher-performance applications or other job mixes. BBN has added special calls so that a programmer can create processes or allocate memory on specific processors, dedicate nodes to particular applications, and dictate how many processors should be used for an application.

Mach 1000 supports BBN's applications library, a development tool for C and Fortran 77 programs that helps programmers to manage system resources and to interface applications to the operating system. The library is called the Uniform System. It provides configuration independence for parallel programs, and creates a single large address space that resembles a familiar uniprocessor development environment. The Uniform System provides dynamic load balancing across all processors for high processor utilization and program efficiency. It also includes a performance-analysis facility for graphically displaying and analyzing program behavior dynamically.

Mach 1000 also supports X Windows, the network-user environment that is becoming a de facto standard. This means that Butterfly programmers can display both text and graphics applications and exchange information between windows. Mach 1000 takes Mach a step further by enabling the system to deal with a nonuniform memory architecture in which it's advantageous to keep some memory references local to the processor board and necessary to refer others through the switch to remote memory.

To take advantage of the capabilities of the new operating system, BBN designers refined the hardware used in the two earlier generations of Butterflies. They managed to push the performance of the Butterfly Plus processor to 2.5 mips per node by integrating 32-bit data and address paths throughout the system. The top performance in the earlier Butterflies is constrained by the 24-bit data path dictated by board architecture and the 24 address pins of the Motorola 68020 microprocessor. The new processor comes with 4 Mbytes of 256-Kbit random-access memory on each processor node, com-



2. NEW NODE. The new processor nodes for the Butterfly system are complete computers with memory and MC68851 memory management units.

pared with 1 Mbyte in the previous version of Butterfly.

In the Butterfly architecture, the processor node is the basic processing element and the Butterfly switch uses techniques similar to packet switching to perform interprocessor communication. BBN uses a 16-MHz Motorola 68020 microprocesser at its full capability and a 68881 floating-point coprocessor, which implements the full IEEE 754 specification for floating-point arithmetic. In addition, BBN will be one of the first computer companies to use the Motorola 68851 memory management unit, placing an MMU in each processor node.

The new GP1000 computer will embody all the advances inherent in the Butterfly Plus technology. The GP1000 is a stand-alone, general-purpose parallel-processing computer that provides up to 4 gigabytes of demand-paged virtual address space. It will be available in single-processor increments for between $10,000 and $11,000 per processor node. BBN executives say the machine is appropriate for a distributed work-station environment in which applications developers want to adapt standard Fortran 77 and C applications to a higher-performance system.

The machine carries out transparent multiprocessing by using the 68851 demand-paged MMU to translate the virtual addresses employed by the processors into the physical addresses used by the processor-node controller. This controller manages switch transactions and memory references transparently, extending the multiprocessing ability of the 68020 by providing a suite of atomic operations. These operations make certain that Adds, Ors, or Ands are protected against interruption during the brief delay when the process must access remote memory via the switch before completing the process.

The memory modules of all the GP1000's processor nodes (as in the earlier Butterfly) collectively and transparently form the system's shared memory. Special circuitry in each processor node automatically sends memory references either directly to local memory or, to maximize performance, to remote memory via the Butterfly switch. The switch hardware remains unchanged, so this mechanism provides a tightly coupled communications network among processors. However, its microcode has been modified to accommodate the full 32-bit data path of the new architecture.

BBN pushed the performance of the Butterfly Plus processor to 2.5 mips per node by integrating 32-bit data and address paths throughout the system

The switch comprises a modular collection of switching nodes that use packet-switching techniques to manage interprocessor communications. Unlike some hypercube networks, the Butterfly switch frees the processors from communications tasks. BBN maintains that the switch approach has advantages over a bus network. Buses are cost-effective for small configurations, but faster buses require more hardware on each processor node, resulting in more complex circuitry. Further, bus contention increases with the addition of each processor. And while crossbar switching reduces contention by providing a separate data bus for each processor and memory module, crossbars grow exponentially in cost and complexity. ☐

For more information, circle 482 on the reader service card.

TRYING TO ANTICIPATE TOMORROW'S INDUSTRY STANDARD

The principal developers of BBN Advanced Computers' new Butterfly family are hoping they've anticipated another industry standard in choosing the Mach 1000 operating system. Gary Roberts, GP1000 product manager, says "Our goal is to forecast what tomorrow's standards will be. Today's standards can become tomorrow's bottlenecks and we don't want to get caught in a bottleneck."

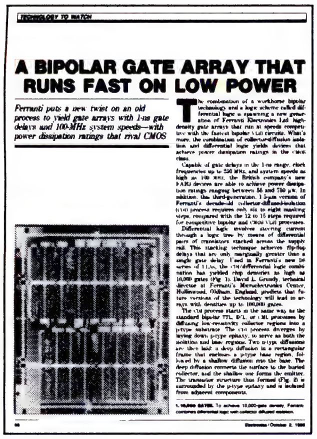
He adds that BBN wants to support standards in general. The safest way to do that with the GP1000 would have been to choose Berkeley Unix 4.3 as an operating system, because of its acceptance in technical and scientific computing, "but it wouldn't have been right for parallel processing."

Tom Blackadar points out that there's precedent at BBN for such a selection, and hopes it works out as well as an earlier decision. Blackadar is project manager for the new Butterfly systems, and a hardware specialist. He says BBN made a decision to go with the Motorola 68000 for the original Butterfly long before it was available. "The decision then was between the Zilog Z8000 and the 68000, at a time when Motorola really wasn't established in microprocessors. We hope we see the same pattern with the Mach 1000."

The advantage of the Mach operating system, says Carl Howe, director of operating system development, is that it is a true multiprocessing operating system "that gives us an advanced base to build on. Its facilities for handling virtual memory are richer than Berkeley 4.3. We also felt that we'd benefit from an alliance with Carnegie Mellon University [the developers of Mach] and from being part of the Mach community. I think we can contribute to that community, as well." As an example of such a contribution, Howe cites BBN's enhancement of Mach in Mach 1000 to handle nonuniform—local and remote—memory efficiently.

BLACKADAR (left), ROBERTS, and HOWE

UPDATE: FERRANTI IS BUSY WITH ITS BIPOLAR ARRAYS



TECHNOLOGY TO WATCH

A BIPOLAR GATE ARRAY THAT RUNS FAST ON LOW POWER

Ferranti puts a new twist on an old process to yield gate arrays with 1-ns gate delays and 100-MHz system speeds—with power dissipation ratings that rival CMOS

Electronics/October 2, 1986

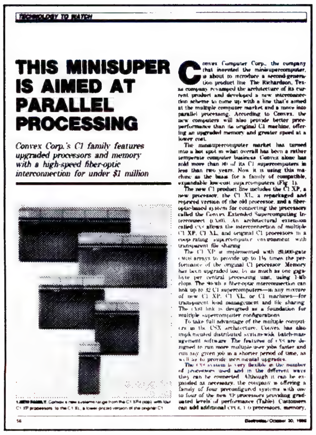
Reaction to Ferranti Interdesign Inc.'s DS family of 2,000- to 10,000-gate bipolar arrays [*Electronics*, Oct. 2, 1986, p. 68] has exceeded the company's most optimistic projections, according to Phillip Pollock, marketing manager for uncommitted logic arrays at the Scotts Valley, Calif., company. Pollock is unwilling to say how many design-ins it has won with the new family, but he will say that the company is postponing the introduction of any higher density versions. "We are finding that with a maximum of 10,000 gates, there are more than enough applications out there to keep us busy," says Pollock. "When the user community signals that it needs higher densities, we are ready to go, but for now our current range of offerings is more than enough."

Built with the company's advanced bipolar process, the DS series is capable of gate delays in the 1-ns range, clock frequencies up to 250 MHz, and system speeds as high as 100 MHz. The gate arrays are fabricated using a 1.5-μm version of the company's collector-diffused-isolation process and implemented using a proprietary circuit technique called differential logic.

This process requires only six to eight masking steps, says Pollock, compared with the 12 to 15 steps for competitive bipolar and CMOS processes. The flexibility of the series has been enhanced through the use of a differential logic scheme involving the selective steering of current through a logic tree by means of differential pairs of transistors stacked across the supply rail, but with flip-flop delays that are only marginally greater than delays for single gates. The technique's inherent common-mode rejection removes problems that are associated with noise, crosstalk, supply-voltage drops and temperature variations. *–Bernard C. Cole*

TECHNOLOGY TO WATCH

UPDATE: ITS XP MINISUPER KEEPS CONVEX ROLLING



TECHNOLOGY TO WATCH

THIS MINISUPER IS AIMED AT PARALLEL PROCESSING

Convex Corp.'s C1 family features upgraded processors and memory with a high-speed fiber-optic interconnection for under $1 million

Electronics/October 30, 1986

A year ago, minisupercomputer pioneer Convex Computer Corp. transformed its uniprocessor C1 machine into a family of products expandable from one to four processors [*Electronics*, Oct. 30, 1986, p. 56]. The Richardson, Texas, company also announced at that time a faster processor for the new C1 XP family featuring 1.5 times the performance of the old one: it is built with 20,000-gate CMOS gate arrays, compared with 8,000-gate arrays in the first CPU. Other enhancements included 1-gigabyte memories and an 80 Mbits/s fiber-optic interconnection to link C1 XP computers in a network.

Now, a year later, most of the systems Convex sells are in the XP family. And "approximately 50% of the XP systems sold so far are the [single-processor] XP1s," says Bob Paluck, president. Most of the rest are XP2s, he says, although the company has just delivered its first four-processor XP4—an upgrade from an XP1—to the Scripps Institute in La Jolla, Calif.

While the first buyers of the Convex C1 systems were primarily research labs in industry, government, and universities, now commercial customers are starting to get in on the act. Paluck reports that in the last quarter, the company sold several systems to commercial users.

But the three biggest application markets remain structural analysis, signal and image processing by government and aerospace companies, and geophysical exploration. The most promising emerging market, says Paluck, is in computational chemistry. "We see lots of action [there]; we offer all the key [applications] packages [for computational chemistry]."

Indeed, Convex has worked with third-party application vendors to put up about a dozen chemistry applications. These were among more than 20 such third-party applications Convex added in its last quarter. "We will have about 200 third-party applications up by the end of the year, up from 100 at the beginning of the year," says Paluck.

With these applications running on C1 machines, customers are getting a lot more work done. Paluck quotes a West German client in computational chemistry as saying that the C1 system allows one organic chemist to design up to 12 new organic compounds each week, whereas he was lucky to do 12 per year before.

Another trend noted by Paluck is the increased use of the large main memories made available last year. These big memories are most used today in the geophysical and computational-fluid-dynamics applications. "A large main memory allows users to do three-dimensional modeling instead of 2-d, and to be able to simulate much larger models, such as a whole airplane—even one as big as a 747," Paluck says.

The one new item introduced a year ago that is not getting much use yet is the fiber-optic link. According to Paluck, most of the hardware connections among Convex systems use Ethernet links. *–Tom Manuel*

TECHNOLOGY TO WATCH

UPDATE: IDT REWORKS ITS 32-BIT-SLICE PROCESSOR

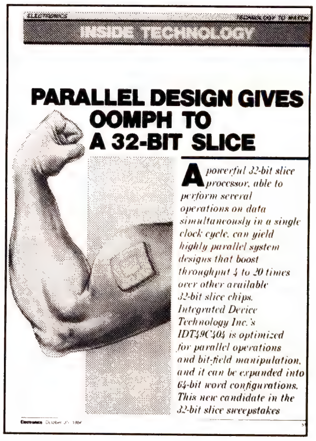
Integrated Device Technology Inc. went back to the drawing board last year shortly after it announced that it had just produced samples of the first parts for its new 49C404, a "breakthrough" microprogrammable 32-bit-slice processor [*Electronics,* Oct. 30, 1986, p. 51]. The Santa Clara, Calif., company then spent a year developing a higher-performance version, which is now scheduled for introduction in the first quarter of 1988.

"When we looked at the competitive situation, it was clear to us that to establish a presence in the marketplace we'd have to go into redesign on the part immediately, to generate an even faster follow-on," says Larry Jordan, vice president of marketing at IDT.

That meant the company had to decide whether to go to market with the original 49C404, which was supposed to compete with 32-bit building block designs from the likes of Advanced Micro Devices Inc. and Texas Instruments Inc. It chose not to, figuring the money needed to launch the product would be better spent supporting existing products.

The new processor will boast instruction-execution cycle times in the 40- to 60-ns range, versus about 80 to 120 ns for the earlier part. The speed improvement, Jordan says, is achieved through architectural and circuit improvements combined with an aggressive new CMOS process with 1.0-μm geometries, compared with the original's 2-μm CMOS process.

Otherwise, the newer version incorporates many of the features of the earlier one. Among them are a register file with four output ports and three input ports, an on-board funnel shifter that is linked sequentially to an eight-function, 32-bit arithmetic logic unit. Its three-bus architecture is optimized for bidirectional operations. These features allow shift, rotate, mask and merge operations in a single clock cycle, the company says, rather than in separate cycles as in competitive designs. *–Bernard C. Cole*


INSIDE TECHNOLOGY

PARALLEL DESIGN GIVES OOMPH TO A 32-BIT SLICE

A powerful 32-bit slice processor, able to perform several operations on data simultaneously in a single clock cycle, can yield highly parallel system designs that boost throughput 4 to 20 times over other available 32-bit slice chips. Integrated Device Technology Inc.'s IDT49C404 is optimized for parallel operations and bit-field manipulation, and it can be expanded into 64-bit word configurations. This new candidate in the 32-bit slice sweepstakes

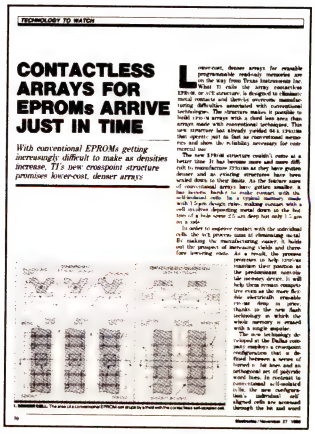
TECHNOLOGY TO WATCH

UPDATE: TI'S 1-MBIT EPROM TO USE CONTACTLESS ARRAY

Denser, lower-cost arrays for erasable programmable read-only memories were the promise held out a year ago by Texas Instruments Inc. for its contactless crosspoint EPROM array structure, dubbed ACE [*Electronics,* Nov. 27, 1986, p. 70]. Now, TI says that prototype EPROMs built with ACE have performed so well over the past year that it is preparing to launch a 1-Mbit EPROM family using the process. The devices will debut in the first quarter of 1988, says Pradeep Shah, manager of advanced nonvolatile product development in TI's MOS memory division, Houston.

ACE's contactless structure overcomes the problem of using metal to make contact with the self-isolated cells of the memory array. Instead, the cells are accessed through buried n+ bit lines and orthogonal polycide word lines. Isolation between the bit lines and the word lines is provided by a layer of thick oxide grown over the n+ layer. Isolation from one bit line to the next is achieved by ion implantation. In practice, TI does use some metal, to reduce bit-line resistance. Expected improvements in polycides will eliminate all of the metal, Shah says.

The first product is the 64 K by 16 bit TMS27C210, which is currently undergoing qualification tests. This device will not quite deliver on the promise of greater density: checking in at 86,000 square mils, the chip is comparable in size to conventional 1-Mbit EPROMs. But Shah points out that the chip will be made with relatively loose 1.5-μm design rules, while competitive products use 1.2-μm rules to achieve the same density. As to cost, Shah says the ACE process has the potential for greatly reducing the chip size, a major cost factor. Prices have not been set. TI is also developing a 128 K by 8 bit version, the TMS27C010. *–Samuel Weber*


TECHNOLOGY TO WATCH

CONTACTLESS ARRAYS FOR EPROMs ARRIVE JUST IN TIME

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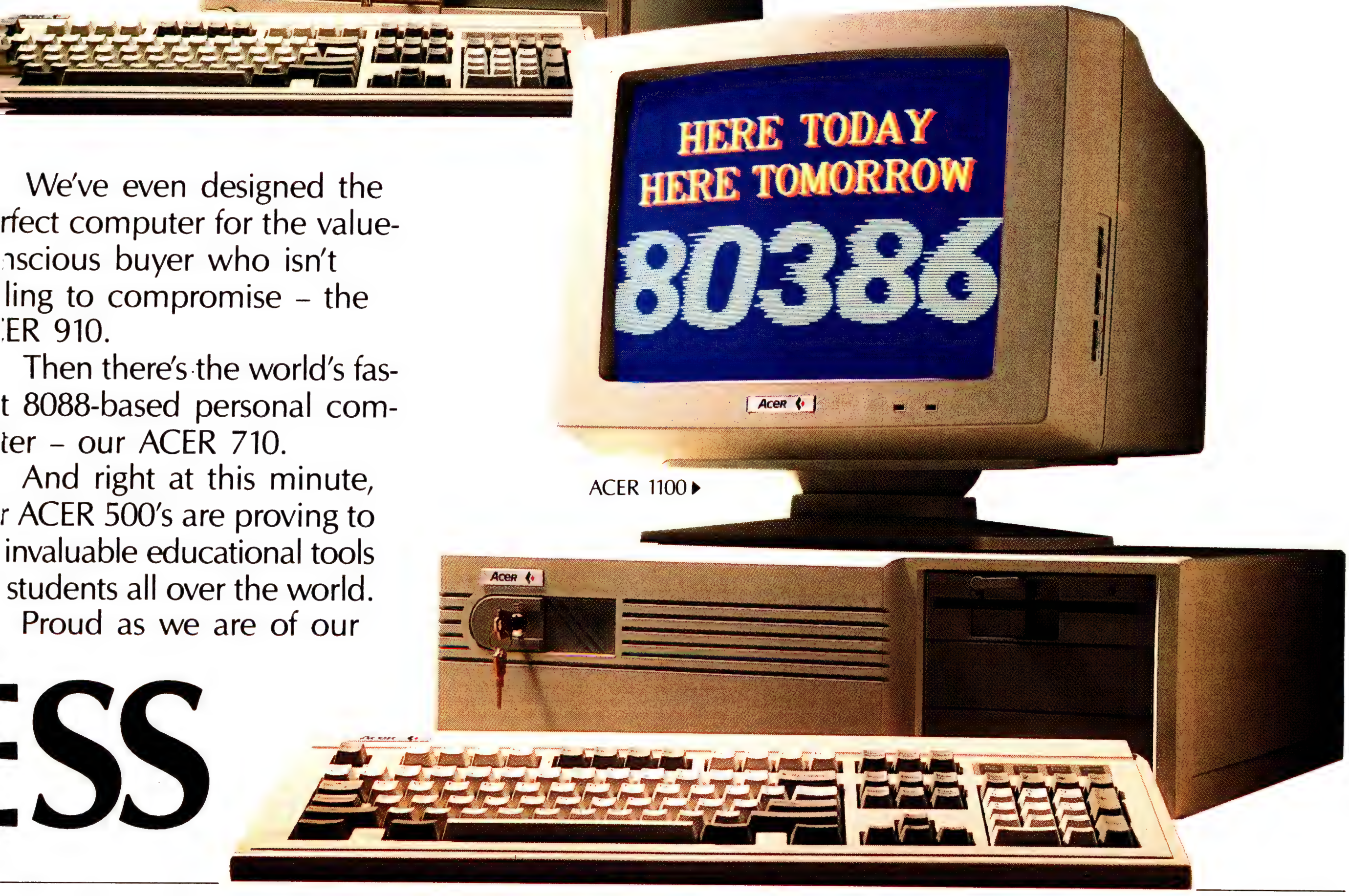

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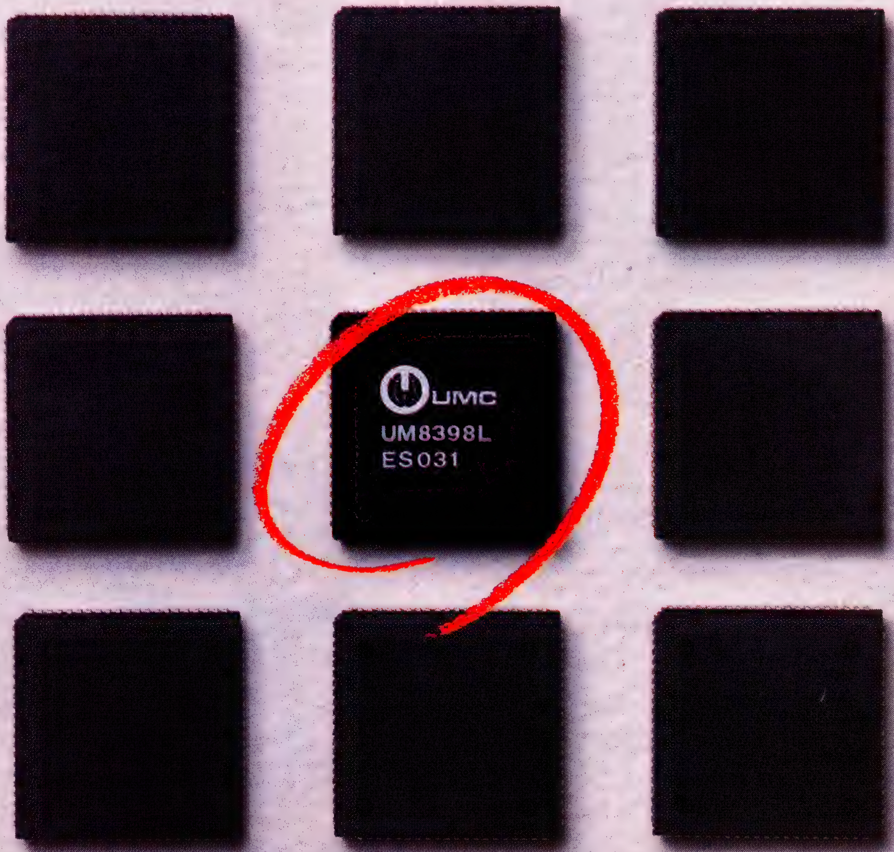

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MILITARY/AEROSPACE NEWSLETTER

NOW ADA HAS A REAL-TIME OPERATING SYSTEM

The biggest problem in writing application software in Ada, the mandated high-level language for all U. S. military computers, has always been the lack of a real-time operating system that supports it. Now Ready Systems, a Menlo Park, Calif., software firm specializing in real-time operating systems, has joined with Telesoft, a supplier of Ada compilers, in an attempt to meet that need with RTAda. Targeted at embedded mission-critical systems, such as head-up displays, engine controls, and weaponry, RTAda draws heavily on VRTX, Ready Systems' flagship real-time product. Ready Systems is expected to unveil RTAda and RTAda-1750A, a development system aimed at Mil Std 1750A computer applications, at ADA Expo in Boston Dec. 8-11. ☐

TRW SEES FIRST SILICON ON A PHASE 2 VHSIC MEMORY CHIP

The first silicon to come out of TRW Inc.'s Phase 2 Very High Speed Integrated Circuits program is a memory chip built to demonstrate self-testing and self-configuring functions. But TRW's Electronic Systems Group in Redondo Beach, Calif., acknowledges that the device does not boast the 0.5-μm dimensions called for by VHSIC Phase 2. Instead, it has designed the part with the 1.25-μm lines developed for Phase 1. The reason: a delivery delay for the Perkin-Elmer Corp. Aebele 150 direct-write electron-beam system needed to reach 0.5-μm dimensions. The design called for a 725-Kbit usable capacity, but on-chip cell yields were high enough to give a 1.2-Mbit capacity, says Thomas A. Zimmerman, director of the company's VHSIC program. Despite the delivery delay for the e-beam system, Zimmerman says TRW expects to meet 1989 Phase 2 delivery deadlines. ☐

DARPA SCRAMBLES TO FIND THE MONEY FOR SUPERCONDUCTOR RESEARCH

The Defense Advance Research Projects Agency is looking to award contracts for high-temperature superconductor research in early January—but just where the funding will come from is still up in the air. Richard A. Reynolds, director of Darpa's Defense Sciences Office, says the agency is willing to redirect about $50 million of its own funds over the next three years, but that won't be enough. He figures that a minimum of $20 million a year for as many as 20 years or more will be necessary to put superconductors in the forefront of useful military technologies. There is hope that one well-funded defense program might be interested in kicking in some money: "It now appears that the Strategic Defense Initiative Organization may join the program," Reynolds says. The proposals cover applications ranging from thin-films for microelectronics and infrared detection to bulk magnets for sophisticated weaponry. ☐

UNITED TECHNOLOGIES TO ADD LINEAR BIPOLAR CHIPS TO ITS MILITARY LINE

The United Technologies Microelectronics Center, Colorado Springs, Colo., is adding high-voltage linear bipolar circuits to its line of digital CMOS military-standard products. UTMC plans to supply prototypes in next year's first quarter on what are billed as the first standard monolithic transceiver circuits developed for the Air Force Mil Std 1553A and 1553B bus. The UT63M1XX family will be offered in both single- and dual-channel versions designed to meet 1,553 redundancy requirements. The dual-channel version features custom packaging with two physically and electrically isolated cavities, each housing one of the transceiver chips. UTMC says the devices will dissipate less than half the power of conventional hybrid implementations, which typically require a 3.6- to 4.4-W duty cycle. The UT63M1XX family is planned for production in next year's third quarter. ☐

OCTOBER 29, 1987

MILITARY/AEROSPACE NEWSLETTER

HONEYWELL WILL BE FIRST TO PRODUCE RAD-HARD 64-KBIT SRAMs

Honeywell Inc. is pushing the limit on radiation-hardened, high-performance military static random-access memories with three new 64-Kbit SRAMs that should emerge next year. The Minneapolis company's Solid State Electronics Division is planning first-quarter prototype deliveries and third-quarter production on the HC6264R, 8K-by-8 chip built in 1.2μm CMOS technology. Typical access times will be 80 ns for the part, which is being billed as the first 64-Kbit SRAM to meet strategic radiation-hardness levels as defined by the Transient Radiation Effects on Electronics Group, a joint military services organization. Total-dose tolerance will be specified at 1 megarad, although early versions of the chip have withstood up to 50 megarads in testing. Prototypes of two more 64-Kbit SRAMs, this time with 40-ns access times, are expected by fall of 1988. □

HONEYWELL'S VHSIC-BASED 1750A CHIP SET REACHES THE FOUNDRY

Honeywell Inc. is polishing off its design work and moving to the foundry with the first of the five chips that make up the Generic VHSIC Spaceborne Computer. The GVSC, which uses CMOS chip technology developed under the first phase of the Very High Speed Integrated Circuits Program, is a radiation-hardened implementation of the 16-bit Mil Std 1750A architecture. It could become a critical part of several Strategic Defense Initiative programs. A ranking technical official at Honeywell's Space and Strategic Avionics Division in Clearwater, Fla., says the first two designs went to the company's Plymouth, Minn., foundry in October and the remaining three will be there by December. First-pass test chips are expected in February, and initial volumes of the 1.25-μm CMOS parts should roll off the line in April. Honeywell's GVSC will boast worst-case throughput of 3.7 million instructions per second, 23% faster than the worst-case performance specified by the Air Force contract. □

ASU DEVELOPS AN EXPERT SYSTEM FOR GaAs CRYSTAL GROWTH . . .

The Semiconductor Materials Laboratory at Arizona State University has developed a fully automated system for growing gallium arsenide crystals that ups yields while virtually removing the need for a system operator. Under funding from the Defense Advanced Research Projects Agency, ASU researchers have developed an expert system and a digital computer that can take a typical Cambridge Instruments Co. 358 growth system and boost yield by almost 50%, while cutting operator time from 22 hours to just over 2 min. Lab director Gunther Schwuttke says he is getting single-crystal yields of better than 70% and controlling the diameter of his wafers to within 1 mm. Schwuttke says the improvements should become available to U. S. customers through the San Diego, Calif., equipment company by mid-1988. □

. . . WHILE MIT SEEKS TO USE THEORY TO CONTROL GaAs GROWTH

MIT theorists are using fluid-dynamics calculations, heat-transfer calculations, and advanced control theory to develop a gallium arsenide crystal-growth system that will be based not on human knowledge, as are conventional expert systems, but rather on theoretical laws and principles. Funded by the Defense Advanced Research Projects Agency, the goal of the program "is to minimize or eliminate expert systems and have the theoretical model control, through a computer, the growth process," says Gus Witt, the professor of material science and engineering running the program. Key to the effort is the development of a heat pipe, a housing that, residing inside a reaction furnace, maintains temperature levels throughout the cavity far more accurately than is possible with conventional furnaces. □

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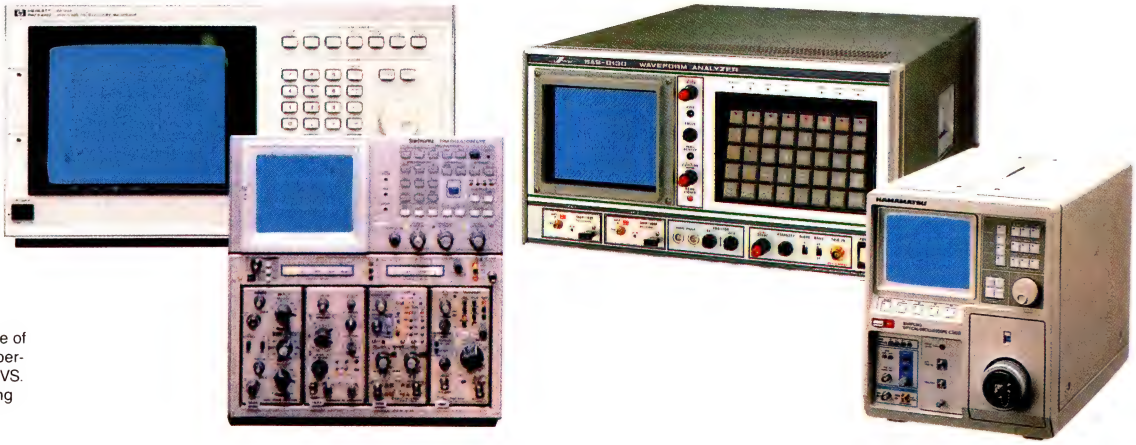

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ZYMOS SIX-CHIP SET CUTS COST AND CHIP COUNT FOR PC AT CLONE

POACH/ATF-B FAMILY ELIMINATES SUPPLEMENTARY TTL LOGIC

Zymos Corp. is wooing makers of IBM Corp. Personal Computer AT compatibles with a chip set that would enable them to build 16-MHz performance for about $300 in an assembled motherboard—that's $25 less than competitors' chip sets. Pricing on the six-chip set is $90. A 12-MHz version costs $75.

Harnessed to CMOS versions of Intel Corp.'s 80286 microprocessor, 80287 math coprocessor, 8042 keyboard controller, and 512 Kbytes of system memory, the six-chip Poach/ATF-B set requires no additional TTL parts to implement an AT system. The solution is based on the Sunnyvale, Calif., company's extensive library of standard-cell "supercells." It offers a total component count of 29 chips—including 20 memory chips—compared to more than 40 chips for the competition. Two more Poach chips can be added to make the design compatible with Intel's 32-bit 80386 microprocessor.

PS/2 RIVAL. Clonemakers can even use the chip set to compete successfully on a cost/performance basis with IBM's recently introduced Personal System/2 Model 30, says Robert G. Andrews, director of technical marketing. This is possible, he explains, because the Model 30 does not support IBM's Micro Channel architecture or its Video Graphics Adapter standard. Several Taiwanese companies, he says, are already hard at work on AT clones that aim at matching the Model 30's functionality.

Operating system compatiblity presents no problem because the Zymos chips support Microsoft Corp.'s MS-DOS and OS/2, the company says.

Zymos started by upgrading its Poach 1 and 2 chips, introduced in 1985. Zymos put a lot of effort into keeping the pinouts similar to reduce the time AT designers need to adapt the new chips, says Andrews, but the earlier chips ran at 8 MHz, and additional logic had to be added to bring the enhanced versions up to 16 MHz.

The update of the Poach 1 is the Poach 7. It performs system clocking and control functions, including clock-switch logic that is needed to maintain 100% AT compatibility. Since AT expansion boards run at 8 MHz, the Poach system must have the capability of slowing itself by 8 MHz when addressing an expansion board, says Andrews. In addition to the new logic, Poach 7 also uses Zymos supercells to replace five chips on the original AT motherboard: two Intel 8259A programmable-interrupt controllers, an 82288 bus controller, an 82284 clock generator, and a Motorola Corp. 6818 real-time clock/CMOS random-access memory to hold the date and time as well as configuration data.

ZYMOS CHIPS TAKE OVER PC AT FUNCTIONS

POACH 7	POACH 8	POACH 10
SYSTEM CLOCKING AND CONTROL, INCLUDING CLOCK-SWITCH LOGIC REPLACES 8259As (TWO); 82288; 82284; 6818	DIRECT-MEMORY-ACCESS OPERATIONS, INCLUDING TIMER-COUNTER PERIPHERALS REPLACES 8237As (TWO); 8254; 74612; 8284	ADDRESS-BUS BUFFERS
POACH 11	**POACH 12**	**POACH 13**
DATA-BUS BUFFERS PARITY-GENERATION LOGIC	MEMORY CONTROL: • CONFIGURATION • PAGED, INTERLEAVED SUPPORT • BURST-MODE REFRESH • WAIT-STATE CONTROL • SHADOW-RAM CONTROL • 8-, 16-BIT BIOS SUPPORT	• 1-KBYTE BATTERY-BACKED RAM • SLEEP-MODE CONTROL • REAL-TIME-CLOCK OSCILLATOR • PROGRAMMABLE ADDRESS DECODE • TWO 24-BIT PROGRAMMABLE COUNTERS

MEMORY OPERATIONS. Replacing the Poach 2, the Poach 8 handles direct-memory-access operations, including timer-counter peripherals. It replaces two Intel 8237 programmable DMA controllers, an 8254 programmable interval timer, an 8284 clock generator and driver, and a Texas Instruments Inc. 74613 memory mapper.

Samples of the Poach 7 and 8 chips will be available in mid-November.

The remaining four Poach chips are all new and will be available in sample quantities late in the first quarter of 1988. The Poach 10 chip supports the Lotus-Intel-Microsoft Extended Memory System Version 4 to the system board and to extended memory adapter cards. In other words, it gives the system the ability to address up to 16 Mbytes of memory. The Poach 11 data buffer handles parity generation logic. The Poach 12 memory controller implements memory-control configuration. This chip allows the use of slower, less expensive dynamic RAMs for system memory. Running on a 16-MHz clock, for example, designers can use 120-ns DRAMs and achieve wait-state performance of half of a clock cycle in a two-way interleaved page mode. Using 100-ns DRAMs, the wait-state drops to a tenth of a clock cycle in four-way interleaved page mode.

The Poach 13 targets laptop applications. It includes circuitry that puts the 80286 microprocessor in standby mode to extend battery life. It can actually put the laptop to sleep between keystrokes, according to Andrews. The Poach 13 also includes 1 Kbyte of battery-backed RAM, which holds system information in memory when the laptop is in the standby mode.

Besides high-performance ATs and laptops, the Poach/ATF-B fits applications such as high-integration, small-footprint desktop AT systems; PC AT-based terminals; and single-board computers.

– *Jack Shandle*

Zymos Corp., 477 N. Mathilda Ave., Sunnyvale, Calif. 94088
Phone (408) 730-5400 [Circle 360]

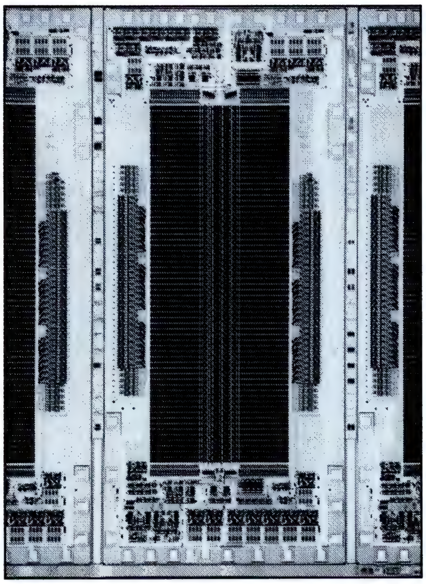
CMOS FIFO MEMORY CHIP RUNS AT 40 MHz

The latest first-in, first-out CMOS memories from Thomson Components-Mostek Corp. use asynchronous read/write operation and a pipeline architecture to deliver cycle times of 40 MHz, almost double the speed of its competitors.

The 4505 FIFOs are intended for applications that move data quickly on square-wave clocks. The parts specifically target digitized video and audio systems, image processing, analog-to-digital and digital-to-analog converters, fast data links, radar-return sampling systems, and data-tracing functions.

TWO INPUTS. The 1,024-by-5-bit MK4505 hits such high speeds by implementing asynchronous operation. Two independent free-running input signals—each boasting 15-ns access times—combine to produce a device that equals the speed of a single-port input device running at a 40-MHz clock speed. The peripheral logic controlling the FIFO's static-RAM array performs simultaneous read and writes to dual-port storage cells under asynchronous operation.

"We have partitioned the functions to happen concurrently," says Tom Tyson, memory products marketing manager. "In a regular RAM, you are normally doing all the functions at one [clock cycle]." The pipeline architecture of the 4505 parts enables them to perform some of the address-related functions while other bits are being accessed or stored.



FAST. The MK4505 hits 40 MHz speeds by using two independent input signals.

The company is fielding two versions of the device. A 24-pin master 4505 features status flags indicating whether the memory array is full, empty, half full, almost full, or almost empty. It also has status flags for data-ready and output-valid. A 20-pin version of the 4505 has been configured as a slave FIFO with extra enables for write and read.

The devices were configured in a by-5-bit organization so they could slip into low-cost 300-mil-wide dual in-line packages with 24 and 20 pins instead of the 600-mil 28-pin DIPs housing competing 1-K-by-9-bit FIFOs, says Tyson. By using a master and slave 4505 pair, users can achieve a 10-bit-wide FIFO configuration that supports a parity bit and an additional control or status bit. The parts are cascadable to any FIFO depth without additional logic. FIFO system width can be increased to more than 40 bits with no additional logic.

NO CORRUPTION. The parts also have internal latches to prevent data corruption from metastable logic states that could result from asynchronous operations, says Ross Smith, the chip's designer. "This chip will take care of those problems for you, which makes it ideal for high-speed systems," he adds.

Processed in Thomson-Mostek's 1.2-μm double-level CMOS technology, the 45,000 mil^2 die has a worst-case power dissipation of 100 mA. The master and slave versions will be available at the end of October in three speed grades: 15 ns, 20 ns (30-MHz or 33-ns cycle times), and 25 ns (20-MHz or 50-ns cycles). In quantities of 100 parts, the 40-MHz master sells for $53.81 each. The 30-MHz master is priced at $44.89 each and the 20-MHz part costs $37.41. In similar quantities, the 40-MHz 20-pin slave is priced at $48.43 each for 40-MHz, $40.40 each for 30-MHz, and $37.41 for 20-MHz.

– J. Robert Lineback

Thomson Components-Mostek Corp., 1310 Electronics Dr., Carrollton, Texas 75006. Phone (214) 466-6000 [Circle 361]

XILINX HIKES PLD DENSITY BY 4X TO GET 9,000 GATES

Xilinx Inc. is boosting the density of its programmable logic devices almost fourfold with a 9,000-gate PLD fabricated in the company's proprietary logic-cell array based on a static random-access-memory technology. The XC3090 will become available in sample quantities in December, following hard on the heels of the San Jose, Calif., company's 2,400-gate XC3020 [*Electronics*, September 17, 1987, p. 69].

Unlike the restrictive AND/OR-plane architecture used in most PLDs, the 3090 has a gate-array-like architecture that allows high gate utilization even at the 9,000-gate level, says Wes Patterson, Xilinx executive vice president. A new 1.2-μm double-layer metal CMOS process results in circuit performances equal to gate arrays in many typical applications, he says. Moreover, claims Patterson, the XC3090 breaks all previous barriers for programmable logic with its equivalent of 9,000 two-input NAND gates in the form of 640 user-definable logic functions and 928 flip-flops. It also features 144 user-programmable input/output pins.

A key strategy in the introduction of this second generation of high-density PLDs was to enter the market with low- and high-end devices—the 2,400- and 9,000-gate parts—says Patterson. By using a modular design, the company then can fill in the family with a range of other densities.

"What this means is that the designer can start designing with the larger device and then select the appropriate array size for production," Patterson says. "Changes, both design and marketing, can be accommodated without the inventory risk of mask-programmed devices." Since Xilinx used a modular approach, other members of the family can be generated very quickly. Samples of the entire family should be available during the first half of 1988, says Patterson.

COMPACT. Xilinx uses pin-grid arrays in its new PLDs.

The 2,400-gate XC3020, with 64 logic blocks and 128 user-definable logic functions as well as 256 flip-flops, will be available in volume in the second quarter of 1988. Parts will cost about $20 each in large-quantity purchases. The 9,000-gate XC3090 packaged in 175-pin-grid arrays will also be available in production volumes in the second quarter. Pricing is projected at $200 to $250 each in 1,000-unit lots.

Other devices in the family will include the 3,000-gate XC3030, a 100-logic-block array with 200 user-definable functions, 360 flip-flops, and 80 user-programmable I/O pins; the XC3042, a

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Com/Reg. TM 3Com Corp. IBM/Reg. TM IBM. Corp.

4,200-gate device with 144 logic blocks, 288 user-programmable logic functions, 480 flip-flops, and 96 programmable I/O functions; and the XC3064, a 6,400-gate device with 224 logic blocks, 448 logic functions, 688 flip-flops, and 120 programmable I/O pins.

Schematic entry for the 3000 family is available on the Dash and Schema II development systems from FutureNet Division of Data I/O Corp., Chatsworth, Calif. By the end of the year the arrays will be supported on most major computer-aided-design work stations, says Patterson. *– Bernard C. Cole*

Xilinx Inc., 2069 Hamilton Ave., San Jose, Calif., 95125.
Phone (408) 559-7778 [Circle 362]

POWER-MONITORING CHIPS REPLACE UP TO 10 ICs

Each chip in the Maxim Integrated Products' MAX690 CMOS family replaces about 10 integrated circuits and discrete components that monitor system power and switch main memory to battery backup during failures. They also perform housekeeping functions common in microprocessor-based equipment, which earlier monitor chips don't do.

The Sunnyvale, Calif., company is promoting the MAX690 family as a second generation of supervisory IC for microprocessor-system battery backup. Applications include real-time control, programmable controllers, aerospace and automotive electronics, and intelligent instruments, the company says.

WATCHDOG. In addition to power-failure detection and battery-backup control circuits, the MAX690 chips have an on-board watchdog timer that alerts the system whenever errors have hung up microprocessors. The watchdog circuit has timeout periods of 100 ms, and it can be set to wait 1.6 s after power-switching periods. The chips also have an on-chip oscillator. Write-enable protection keeps data from being corrupted whenever system power falls out of acceptable bounds.

The parts pack extra functionality into a reasonable chip size of 116 by 84 mils by using a patented pnp transistor designed for metal-gate CMOS technology, says Brian Gillings, director of strategic planning. The pnp transistors are used in switching power while the device is still running on the normal input power supply. They boast lower differentials between voltages going in and out of the chip than do conventional MOS FETs, says Gillings. If FETs were used for switching, transistors would have to be four times their normal size. In the chip's battery-backup mode, however, FETs are used to switch power.

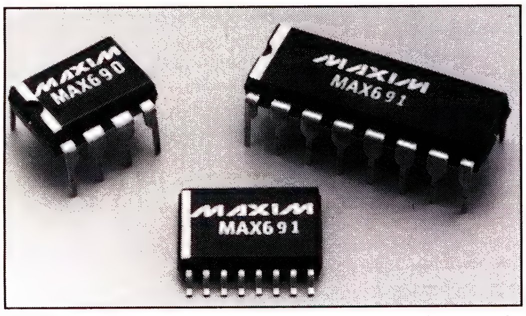
The four members of the 690 line are aimed at what Maxim executives say is a growing number of system applications that team software-running microprocessors with CMOS memories and battery-backed protection modes. The 690 and 692 parts are housed in eight-pin packages, providing four basic functions: reset of output during power-up, power-down, and brownout conditions; battery-backup switchover; reset pulse if watchdog timer has not been toggled; and warning if system power is failing.

The 16-pin 691 and 693 parts provide additional write protection of memory chips, adjustable reset and timeout periods for the watchdog timer, and separate outputs to show battery switchover, low input voltage, or watchdog timeout. In all parts, full hysteresis is used to keep the circuit from trying to switch backup batteries on and off during brownouts, when normal power-supply voltages drop below the trip points.

The 690 and 691 have 4.65-V threshhold detectors, while the 692 and 693 trip at 4.40 V. An uncommitted 1.3-V threshold comparator is available on the 691 and 693 parts for use as a power-fail indicator or for monitoring battery-backup voltage.

The 7-μm metal-gate CMOS chips have a standby current rating of only 1 μA. Maximum power dissipation of the parts are 400 mW in 8-pin plastic dual in-line packages and 600 mW in 16-pin plastic DIPs. In 100-piece quantities, the MAX690/692 sells for $3.30 each. The 16-pin MAX691/693 sells for $3.80 each in similar quantities. Volume shipments began in October. *– J. Robert Lineback*

Maxim Integrated Products, 510 N. Pastoria Ave., Sunnyvale, Calif. 94086. Phone (408) 737-7600
[Circle 364]



THREE CHOICES. Maxim's power monitoring ICs come in 8- and 16-pin DIPs and in a 16-pin surface-mount package.

SEEQ FIELDS 1-MBIT EEPROM MODULE

A 1-Mbit electrically erasable programmable read-only memory from Seeq Technology Inc. offers designers high capacity, low operating currents, and false-write protection.

Packaged in a Jedec-standard, 32-pin dual in-line package, the MM28C1024 is built with four 126-Kbit Seeq 28C256 CMOS chips, a decoder chip, and a decoupling capacitor.

The device can typically be written at a rate of 80 μs/byte. It complies with Mil-Std-883. Available in the first quarter of 1988, the device will cost $17.50 each in 100-unit purchases.

Seeq Technology Inc., 1849 Fortune Dr., San Jose, Calif. 95131.
Phone (408) 432-7400 [Circle 385]

MULTIPLIERS BOAST 35-ns MATH SPEED

A CMOS family of 8-, 12-, and 16-bit multipliers from Logic Devices Inc. uses 1.8-μm technology and improved architecture to form products in 35 ns—half the time competing devices take.

The architecture uses a nonmultiplexed output structure, and that allows the product to be read in a single step.

The 16-bit LMU18 in an 84-pin surface-mount or pin-grid package multiplies two 16-bit inputs and generates a 32-bit output. It costs $30.53 each in 100-unit quantities. The 12-bit LMU12 costs $22.29. The 8-bit LMU008, available in dual in-line plastic packages, ceramic packages, and surface-mount packages, costs $17.06 each.

Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, Calif. 94086.
Phone (408) 720-8630 [Circle 386]

ANALOG SWITCH IS FIVE TIMES FASTER

Siliconix Inc.'s DG411 analog switch offers five times faster switching than the company's industry-standard DG211—and its 0.25-nA leakage current is one fourth that of the DG211.

Fabricated with the company's proprietary high-voltage silicon-gate process, the DG411 boasts a 175-ns switching speed. Low power dissipation of 35 μW maximum allows the chip to be used in remote, battery-powered applications.

Samples are available now with production quantities scheduled for delivery in December.

In 100-piece purchases, the chip costs $3.15 each in plastic dual in-line packages, $3.85 each in small-outline packages, and $7.25 each in ceramic DIPs.

Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, Calif. 94054.
Phone (408) 988-8000 [Circle 367]

5¼-IN. DRIVE STORES 765 MBYTES AT ONLY $3 PER MILLION BYTES

MICROPOLIS 16-MS DRIVE UNDERCUTS COMPETITION BY 40%

Micropolis Corp.'s 1560/1580 series of 5¼-in. Winchester disk drives delivers 16-ms access times and 765-Mbytes capacity in the same package size as 380-Mbyte drives. And the drives are priced at $3 per Mbyte in quantity purchases, a cost the Chatsworth, Calif., company claims is about 40% below that of its only competitor.

At this capacity level, the drives join a select circle occupied by only one other product: the 765-Mbyte, 18-ms-access-time Model XT8760 drives that Maxtor Corp. announced a year ago. The cost per megabyte of the XT8760 is a little less than $5, says Maxtor, of San Jose, Calif.

To round out its upgraded offerings while also addressing the threat from 3½-in drives, Micropolis is also introducing a series of half-height, 5¼-in. drives that store from 85 to 182 Mbytes.

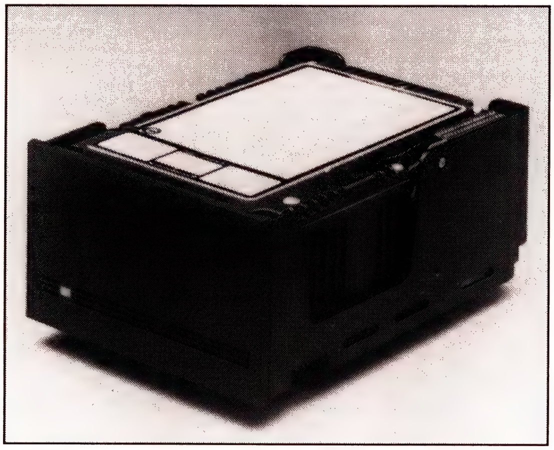
Although the new 765-Mbyte drives basically follow the same technology as their 380-Mbyte predecessors, design engineers made significant improvements to attain the increased performance and capacity. The drives can transfer data at up to 15 MHz, for example, compared with a 10-MHz rate for the previous models. Also, the company has boosted track density from about 1,000 tracks/in. to 1,400—a 40% increase.

INTERFACES. Users may choose either the Enhanced System Device Interface or the synchronous Small Computer System Interface. With the 15-MHz data-transfer rate, the SCSI interface can transfer data at 4.0 Mbytes/s; the rate for ESDI is 1.88 Mbytes/s.

The SCSI interface supports either single-ended or differential interconnection. Reduced command overhead and the drive's 64-Kbyte buffer and read-ahead feature also help speed response. Average seek time with either interface is 16 ms, which Micropolis claims is among the fastest on the market.

The new drive not only targets original-equipment manufacturers incorporating 5¼-in. drives in their products, but also those using larger (8-, 9-, or 14-in. form factor) drives in mini- and mainframe computers, says Chet Baffa, senior vice president of sales and marketing. "The new Micropolis series compares favorably with larger-diameter drives now used for applications where data is frequently accessed," he says.

While Micropolis and Maxtor are now apparently the only companies offering 765-Mbyte drives, they won't be alone for long, predicts Robert Katzive, vice president of Disk/Trend Inc., Mountain View, Calif., a consultant to the drive business. He notes that some 14 companies presently market drives of approximately 380 Mbytes, and the marketing pattern for each new drive often resembles that of its predecessor, he says.



SPEEDY. Boasting a 15-MHz data-transfer rate, the 1588-15 with SCSI interface transfers data at 4.0 Mbytes/s.

The history of 5¼-in. drives since appearing on the microcomputer storage scene early this decade is that a new higher-capacity product is introduced at about 18-month intervals. Deliveries are then scheduled to commence about six months later, although delays have become common due to manufacturing troubles stemming from ever-smaller tolerances.

The likely demand for 765-Mbyte-level drives is not yet clear, since there are no solid data yet. But Disk/Trend projects a burgeoning market for larger-capacity drives. In 1987, the firm says, some 75,000 300-to-500 Mbyte drives will be sold. In 1988, that figure will spiral to 360,000 units.

Micropolis's new drives are specified at an average of 30,000 hours mean time between failure. For service, all boards and mechanical fixtures are individually replaceable units, with no adjustments required. Consequently, the company says that mean time to repair is only 15 min.

Sample drives for evaluation will be ready during the second quarter of next year. Price for the SCSI model, the 1588-15, will be $2,395; for the ESDI unit, the 1568-15, $2,295. These prices are for quantities of 2,500.

Micropolis is also fielding its half-height 1650/1670 series of 5¼-in. drives that store from 85 to 182 Mbytes to target a market niche served by 3½-in. units. The appeal to microcomputer OEMs comes from higher performance—16 ms seek times—and capacities well above 100 Mbytes, which are generally not offered by the smaller drives, say Micropolis executives. "The new 1650/1670 series provides the best balance of form factor, cost, capacity, and performance—and in addition, a growth path to higher capacities not available with smaller drives," says Baffa.

The series is equipped with either the ESDI or SCSI interface and features a newly designed actuator that provides the 16-ms seek performance. On-track head positioning is maintained by a dedicated digital servo system that is based on an advanced digital signal processor, which compensates for variations of components. Data transfer is 10 Mbytes/s. Mean time between failure is 35,000 hours.

Evaluation units will be available in February, with quantity deliveries scheduled for April. Price of the ESDI model 1654 is set at $1,095. The model 1674 with an SCSI interface will sell for $1,165. Both prices are for 1,000-unit quantities.

– Larry Waller

Micropolis Corp., 21123 Nordhoff St.,
Chatsworth, Calif. 91311.
Phone (818) 709-3305 [Circle 340]

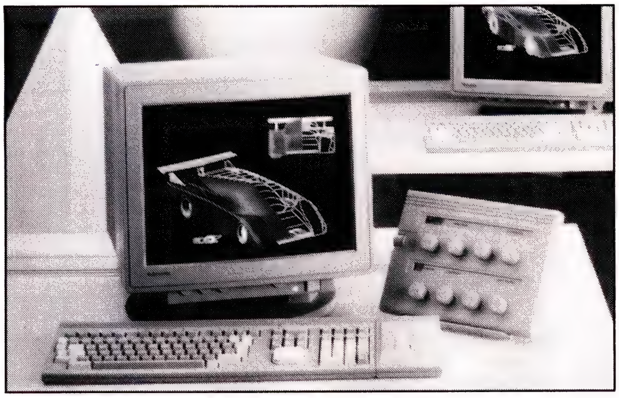
COMDEX/Fall '87

More than 1,300 exhibitors will crowd the floor of the Las Vegas Convention Center Nov. 2 through 6 for the Comdex/Fall '87 show to show the latest applications and products for the computer industry. This product special section previews some of the most exciting products, including leading-edge disk drives, work stations, graphics-display controllers, and data cartridges.

TEK CLAIMS TOP GRAPHICS THROUGHPUT

Graphics performance ranging from bit-mapped monochrome at the low end to 340,000 three-dimensional vectors/s drawing speed and color shading at the high end is offered by Tektronix Inc.'s 4300 Series of Unix-based work stations.

On the top performance rung are two 4330 three-dimensional color work stations that achieve the fastest graphics throughput of any stand-alone work station now on the market, says the Beaverton, Ore.-based company.



CONCURRENT. Tektronix's 4330 work stations use a special concurrent-processing architecture to perform critical graphics functions.

A model 4330 3-d shaded-image true-color station runs at drawing speeds of 450,000 2-d vectors/s, 340,000 3-d vectors/s, and 20,000 shaded polygons/s using the Gouraud shading technique. A model 4330 configured for 3-d wire-frame presentation without shading runs at the same vector-drawing speeds. By comparison, competing machines typically produce 150,000 to 200,000 3-d vectors/s and 10,000 to 20,000 shaded polygons/s.

The work stations, which are compatible with the popular Tektronix Plot 10 software, use Motorola Inc.'s 68020 as their basic processors. The high-end models also use special processors in a concurrent-processing architecture to do the critical graphics functions.

TWIN ENGINE. The high-end 4330 machines have a twin-engine architecture—a 20-MHz 68020 central processing unit and a second 68020 running at 16.7 MHz and doing the job of a graphics-control processor. The twin processors communicate over a VMEbus and also through shared memory. The graphics-control processor handles communications and manages the display list, assisted by a concurrent processing engine with several high-performance special processors.

Among them is a picture processor consisting of three concurrent, special-purpose processors to execute graphics instructions. The first of these is a bit-slice engine, a microcoded, 32-bit-wide integer machine that fetches and decodes display-list instructions. The second is the transform engine, a microcoded machine built around a very fast Analog Devices Inc. ADFP3210 and FPALU3221 floating-point chip set. This pipelined engine calculates and applies transforms, does vector clipping, and performs other complex geometric operations. The third is a tiling-engine gate array for frame-buffer addresses.

A separate Z-buffer board performs the complex calculations necessary for hidden-surface removal. The board contains a 16-bit-deep Z-buffer and two custom chips, called plane-equation generators, that calculate intensity values and depth (Z) values for facet rendering.

Finally, multiple frame-buffer controller chips on the frame-buffer board manage the pixels at that level. All 4330 series models come with a 1,280-by-1,024-pixel 16-in. display.

Following the 4330 work stations on the performance scale are the 4320 series models, which are designed for high-performance 2-d graphics and boast drawing speeds of 90,000 2-d vectors/s.

As with the more expensive 3-d systems, the 2-d graphics performance is achieved with a pipelined concurrent architecture, but with lower-performance parts. The 2-d graphics engine is a two-board set comprising a control-processor board and a picture-processor board. The control-processor board has a 68020 graphics controller, custom transform multipliers, and a custom bus fetch-ahead chip. On the picture-processor board, two Advanced Micro Devices Inc. Quad Pixel Data Manager chips serve as a drawing engine. These work stations have 16-in. displays in 1,024-by-768-pixel and 1,280-by-1,024-pixel resolutions, and 19-in. monitors are available as well.

At the low end, the 4310 work stations offer bit-mapped graphics in monochrome, gray-scale, and color work stations. The monochrome display offers 640-by-480-pixel resolution and a 13-in. monitor. Gray-scale and color models come with 19-in. displays offering a resolution of 1,376 by 1,024-pixels.

The work stations are available now. Prices for the 3-d 4330 series models run from $37,500 to $51,500; the midrange 4320s are priced from $23,500 to $37,500; and the low-end 4310s cost $9,995 to $18,950. *– Tom Manuel*

Tektronix Information Display Group, Tektronix Inc., P. O. Box 1000, Wilsonville, Ore. 97070.
Phone (503) 627-7111 [Circle 341]

COLOR-GRAPHICS BOARD HANDLES HIGH RESOLUTION

A new family of bit-mapped display-controllers gets top performance out of high-resolution color monitors while packing all chips on a single board, rather than the multiple boards of competitors. The UDC-2600 series from Univision Technologies Inc. is designed for such applications as solids modeling, medical imaging, and computer-aided design.

The series handles 1,280 by 1,024 pixels with 26 bit planes and a 60-Hz refresh rate for noninterlaced displays. The Burlington, Mass., company achieves this high performance by harnessing a 20-MHz Intel Corp. 82786 display-controller chip with 6 Mbytes of dual-port video memory. Such high-powered chips are needed for high-speed operations such as polygon drawing, line drawing, bit-block transfers, and multifont text generation, says Julius Perl, vice president for engineering.

Dual porting of the video memory permits high-speed access to the host system—an IBM Corp. Personal Computer AT or compatible, or a Sun Microsystems Inc. VMEbus-based work station. Perl says he knows of no other single-board color-graphics controllers for the AT or Sun work stations. The closest rival requires three boards and is more expensive, he says.

An external VSB-bus interface is also provided for linking to an outboard coprocessor or array processor at a rate of 10 Mbytes/s. Perl says those who need very high-speed transfer—such as medical imaging—would use this feature.

The UDC-2600 series displays 16.8 million colors and offers two bits of graphics overlay for annotating graphic images with text, which is common in Landsat satellite-image analysis, for example.

The standard board—2,048 by 1,024 pixels with 8 bit planes of image memory (1,280-by-1,024-pixel resolution)—is priced at $2,495. The maximum configuration—2,048 by 1,024 pixels with 26 bit planes of image memory (1,280-by-1,024-pixel resolution), will sell for $6,995 and requires a daughterboard. Production shipments will begin in December or January. – *Lawrence Curran*

Univision Technologies Inc., 12 Cambridge St., Burlington, Mass. 01803.
Phone (617) 273-5388 Circle 342]

500-MBYTE CARTRIDGE BOOSTS STORAGE 70%

DEI Inc.'s Series II Gold Plus 5¼-in. data cartridges store up to 500 Mbytes—60% to 70% more data than conventional cartridges.

The new cartridges were built to provide backup for Winchester disk drives and as an alternative to IBM Corp. 3480 cartridge-based drives. DEI is also offering 3½-in. MicroTape 2000XL minicartridges that can store 100 Mbytes.

Sample cartridges of both types are available now. Volume production is scheduled to begin in January 1988. Suggested retail prices are $59 for the Series II Gold Plus 1000 cartridges and $35 for the MicroTape 2000XL minicartridges.

DEI Inc., 10170 Sorrento Valley Rd., San Diego, Calif. 92121.
Phone (619) 452-7840 [Circle 345]

WORK STATION RUNS 32 USERS WITH NO LAN

Rexon Business Machines Corp.'s multiuser work-station system is based on Intel Corp.'s 16-MHz 80386 microprocessor and can support up to 32 users concurrently without a local-area network.

The Summit 2000 system uses industry-standard IBM Corp. Personal Computer AT architecture. Its hardware features include a dedicated 32-bit memory bus, a 1.2-Mbyte floppy-disk drive, and a 50-Mbyte fast-access Winchester disk drive.

It has 1 Mbyte of main memory, two 8-bit expansion slots, and six 16-bit expansion slots. On the software side, it uses MS-DOS 3.2 and GW Basic software.

The motherboard is socketed for an Intel 80287 or 80387 coprocessor. The system offers a wide range of configuration options, including disk storage of up to 380 Mbytes, streaming-cartridge

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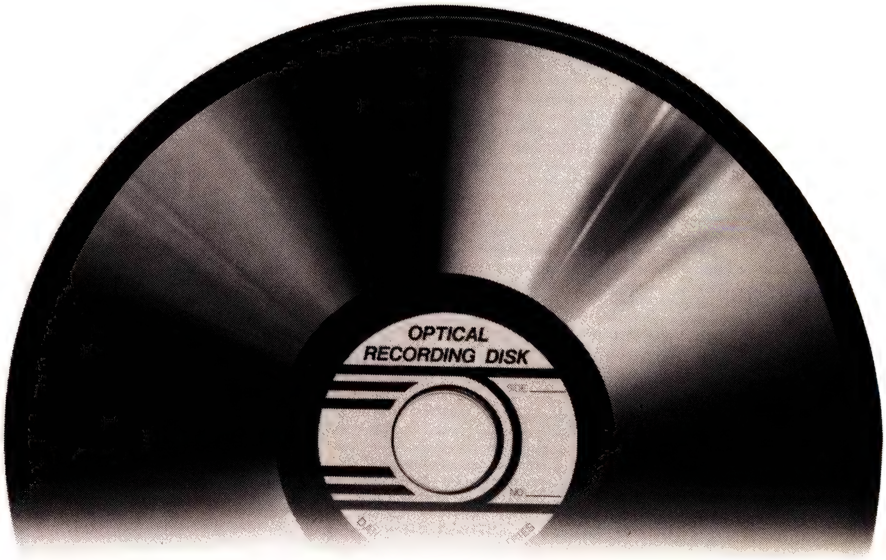

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Telex: 222-4632 DAICEL J Facsimile: [03] 593-2708
Daicel [U.S.A.] Inc.: 611 West 6th Street. Suite 2152 Los Angeles,
CA 90017, U.S.A. Phone: [213] 629-3656/3657
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Colby Instruments, Inc. is a leading manufacturer of very fast pulse generators and clock drivers with pulse repetition rates to 5000MHz and risetimes to 30ps. For further details, contact:

COLBY INSTRUMENTS, INC., 1810 14th Street, Santa Monica, CA 90404. Phone: (213) 450-0261. FAX: (213) 452-0027.

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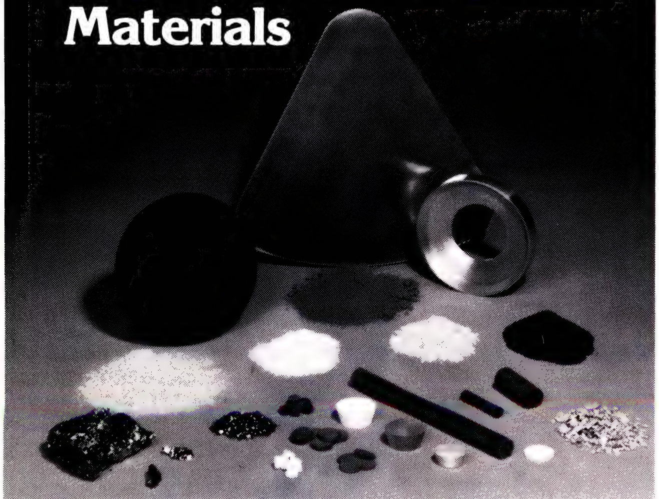

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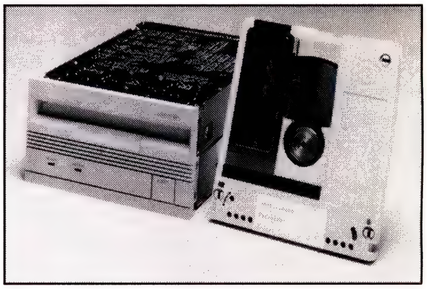
Rexon Business Machines Corp., 3001 Orchard Pkwy., San Jose, Calif. 95134
Phone (213) 641-7110 [Circle 348]

OPTICAL DRIVES USE STANDARD SOFTWARE

Laserdrive Ltd.'s LaserBank 800 optical-disk drive is compatible with magnetic disk drives, eliminating the need for software routines and access methods different from those used for the magnetic units.

As a result, the LaserBank 800 can, without modification, run application software and operating systems developed for Winchester disks.

The optical-disk drive offers 810 Mbytes of storage, access times of 175 ms, and data-transfer rates of 2.78 Mbits/s. In the Winchester mode, it reads, writes, and appears erasable to the user. It also supports a write-once read-many mode.



Available now, single-drive LaserBank subsystems retail for $4,995. Double-sided 810-Mbyte optical cartridges cost $189 retail.

Laserdrive Ltd., 1101 Space Park Dr., Santa Clara, Calif. 95054.
Phone (408) 970-3600 [Circle 346]

ICON COMPUTERS LINK DIVERSE HARDWARE

Icon International Inc.'s new MultiMicro/Mainframe family of computers can link a variety of similar and dissimilar computers and operating systems. Using multiple microprocessors in parallel, the computers can connect personal computers, minicomputers, and mainframes running the Unix, Pick, and MS-DOS operating systems.

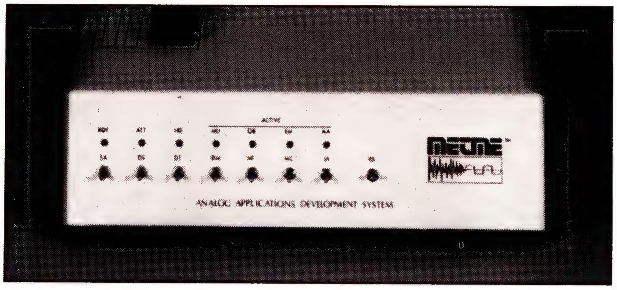
The family includes the Icon 2000 and 3000, which are available now, and the Icon 4000, which will come to market in November. Prices begin at $15,000 for the 1-to-16-user Icon 2000 and at $30,000 for the 16-to-64-user Icon 3000. The Icon 4000 will accommodate 32 to 128 users and will sell for $55,000 and up.

Icon International Inc., 774 South 400 East, Orem, Utah 84058.
Phone (801) 225-6888 [Circle 347]

TOOL LETS DSP DESIGNERS SEE RESULTS IN REAL TIME

METME CUTS UP TO FOUR MONTHS OFF DEVELOPMENT TIME BY ELIMINATING THE NEED TO BUILD PROTOTYPES

A new development tool for digital-signal processing eliminates the need to build DSP prototypes by letting designers and engineers see the real-time results of changes in software or hardware on an oscilloscope plugged into the system's analog input and output port. The Analog Applications Development System—AADS—can reduce the time it takes to design DSP applications by as much as four months, say executives at Metme Corp.



PORTABLE. After software is developed, AADS can be taken into the field with its DSP program stored in battery-backed memory.

The AADS unit allows engineers to "tinker with the DSP algorithms, memory configurations, and analog-interface hardware to explore tradeoffs in performance and price for his specific application," says Robert A. Nimmo, president of Metme. AADS was developed while the St. Louis, Mo., company was developing its own DSP-based analog products. "We believe what has been missing [in DSP development] is a tool that allows engineers to make just a single change or a group of changes and immediately see the effect on the analog signal," Nimmo says.

Metme's AADS unit can be used with an attached IBM Corp. Personal Computer or compatible to implement and examine relatively modest modifications to algorithms prior to embedding them in firmware. In addition, it can also be connected and used with a standard DSP development system for work on complex programs.

The output of a development-system emulator plugs directly into the top of the AADS, which then runs the modified algorithms through its configured hardware and analog interface. Once laboratory work is completed, AADS can be unplugged and taken into the field for trial runs with the developed DSP software safely stored in its battery-backed random-access memory.

The initial version of Metme's AADS contains a DSP engine in the form of a Texas Instruments Inc. TMS32020 or TMS320C25 chip. The development system's analog port can be provided by either a customer-defined interface, a standard codec, or TI's new 32040 DSP front-end chip [*Electronics,* Sept. 3, 1987, p. 150].

Data-conversion circuits in the unit's analog interface can be set at various analog-to-digital and digital-to-analog resolutions or speeds. A range of memory speeds and configurations can also be plugged into the unit, allowing the system engineer to optimize price and performance for a DSP application.

AADS weighs 15 lb and has a power consumption of 15 W at 120 V. The 15-by-13.3-by-4.3 in. unit costs $2,945 with analog interfaces. It is available now.

– J. Robert Lineback

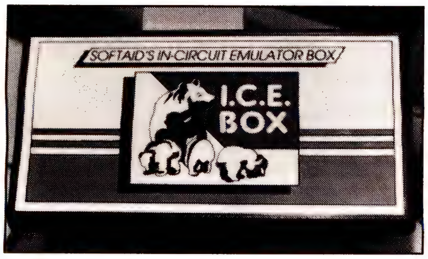
Metme Corp., 4623 Morganford, St. Louis, Mo. 63116.
(800) 445-3830 [Circle 380]

IN-CIRCUIT EMULATOR HANDLES Z280 CHIP

Softaid Inc.'s Z280 Icebox in-circuit emulator supports all the features of Zilog Inc.'s Z280 microprocessor, including its extended input/output addressing, 16-Mbyte address space, memory manager, and 16- and 8-bit modes.

Compatible with any computer or terminal, the emulator runs at full 10-MHz speed without wait states. A 64-Kbit overlay of random-access memory that can be mapped anywhere in the microprocessor's address space speeds application development by functioning like part of the target system.

The Z280 Icebox is compatible with Softaid's TraceAlyzer, a real-time trace-and-performance-analysis system. The Z280 Icebox will be available in November; it will cost $2,500. Available now, TraceAlyzer costs $1,495.



Softaid Inc., 8930 Route 108, Columbia, Md. 21045.
Phone (800) 433-8812 [Circle 385]

CODE GENERATOR IS BASED ON DSP32

By adding a code generator that handles AT&T Co.'s DSP32 floating-point digital-signal processor to its DFDP2 Digital Filter Design Package, Atlanta Signal Processors Inc. lets system designers speed algorithm development.

Unlike general-purpose packages that provide only filter coefficients, DFDP2 generates chip-specific code for implementing digital filters. This means the algorithm runs on the actual hardware rather than in simulation, which allows for real-time testing.

The new code generator enhances the original DFDP2 package, which handles Texas Instrument Inc.'s TMS320 DSP family.

The AT&T DSP32-based code generator retails for $249 and is available now. It is included in the $1,195 DFDP2 package at no extra charge.

Atlanta Signal Processors Inc., 770 Spring St., Atlanta, Ga. 30308.
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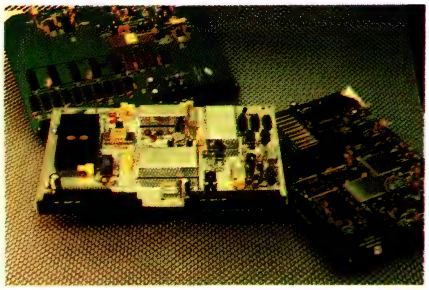

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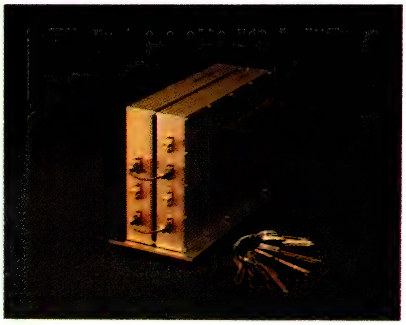

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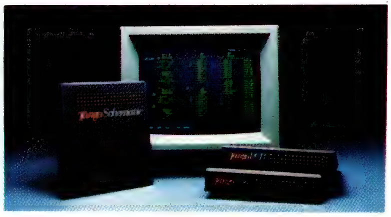

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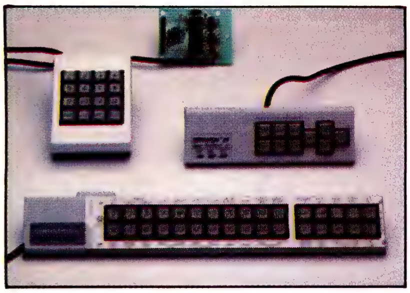

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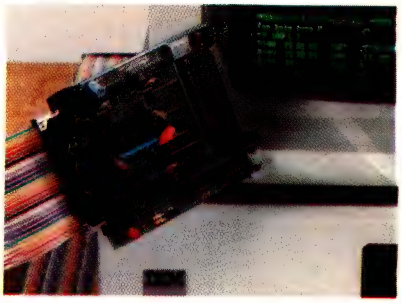

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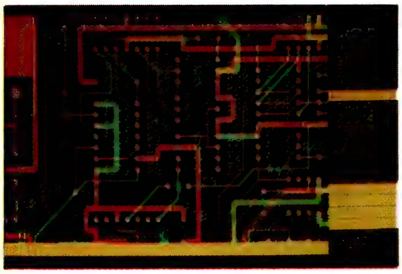

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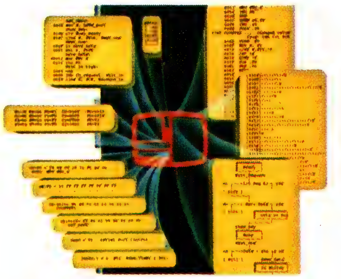

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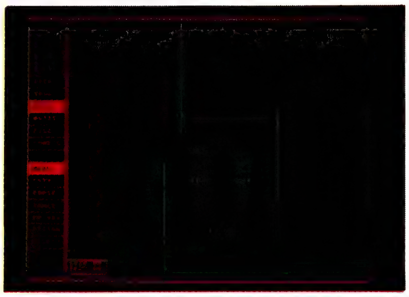

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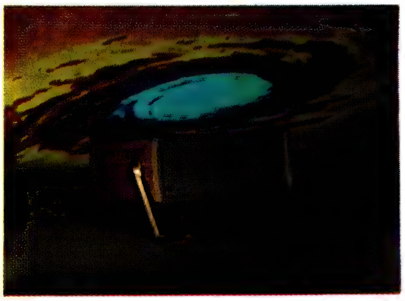

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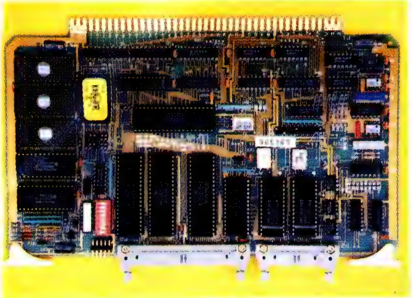

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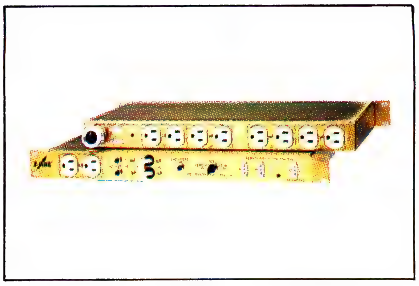

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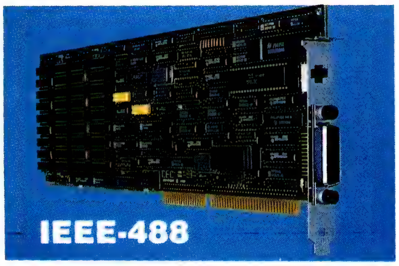

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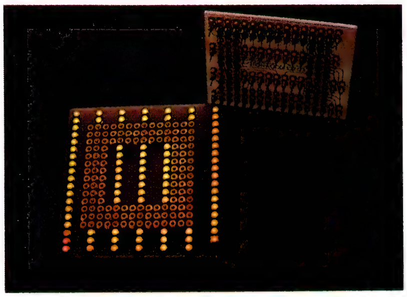

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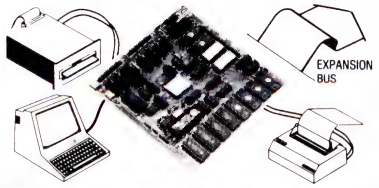

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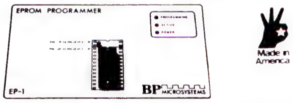

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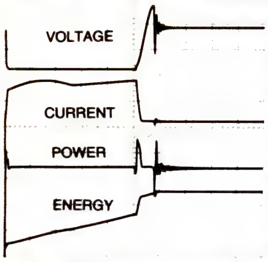

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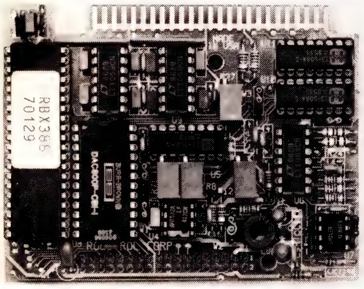

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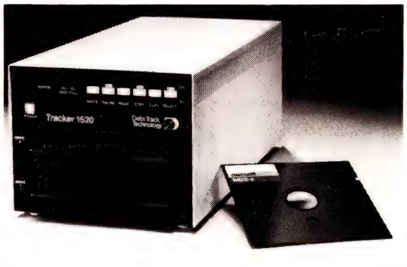

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ELECTRONICS WEEK

SUPERCONDUCTOR CONTACTS IMPROVE

A way to make low-resistance electrical contacts on high-temperature ceramic superconductors has been devised by researchers at the National Bureau of Standards in Boulder, Colo., in collaboration with researchers of the Pittsburgh-based Westinghouse Electric Corp. The contacts' resistance is only 10 $\mu\Omega/\text{cm}^2$, several thousand times lower than that of conventional contacts. Because even a moderate rise in resistive heat can weaken or destroy the ability of the ceramic material to superconduct, the research may help pave the way to commercial applications of the superconducting ceramics.

VERBATIM COATS DISKS WITH TEFLON

Seeking to differentiate its floppy disks from its competition, Verbatim Corp., Sunnyvale, Calif., is bringing out a new line of Teflon-coated 5¼-in. disks. The coating, only a few microns thick, is designed to protect the disks from damage due to finger prints, spills, or scratches. And because the disk surface is so much smoother than conventional floppies, head wear should be reduced, says Frank Ballinson, product manager for the DataLife-Plus disks. The impermeable coating keeps the stain away from the magnetic storage tracks beneath, and actually cleans itself during normal use as it rubs against a specially designed jacket liner inside the disk's plastic envelope. The price is about 15% more than that of uncoated disks, a premium of $3 to $4 per box of 10 disks.

LASA HAS FAST IC-MAKING SYSTEM

LASA Industries Inc., plans to market in the U. S. and Europe its quick-turnaround manufacturing system for application-specific integrated circuits. Lasa, a two-year-old processing equipment manufacturer based in San Jose, Calif., uses a laser semiconductor process called the QT-GA Lasography System. The $3 million, 6-by-3-by-7-ft automated system personalizes uncommitted gate arrays through two layers of metal interconnects under computer control. Lasa claims that QT-GA (quick-turn gate arrays) can deliver working parts in hours. Current ASIC prototyping processes take 6 to 12 weeks.

SEEQ, NATIONAL TEAM ON EEPROMs

National Semiconductor Corp., Santa Clara, Calif., and Seeq Technology Inc., San Jose, Calif., are jointly aiming to dominate the market for high-density flash electrically erasable programmable read-only memories. The two companies have entered a four-year technology licensing and manufacturing pact aimed at producing compatible 256-Kbit to 1-Mbit CMOS flash EEPROMs that would replace slow-programming ultraviolet-light EPROMs. The firms estimate the market for 256-Kbit to 1-Mbit flash EEPROMs will nearly double over the next three years to about $1.2 billion by 1990.

GTE TRIPLES VIDEO CAPACITY OF FIBER

GTE Laboratories Inc., of Stamford, Conn., says it has developed a system that sends 60 broadcast-quality video channels over optical fiber, nearly tripling the previous capacity for analog channels. The development should help to make video transmission by optical fiber cost-effective in the future. In current systems, fewer than half a dozen video signals can be sent digitally and about 24 signals can be sent in analog. Using analog microwave techniques, GTE researchers combined video signals into one microwave signal, which they then impressed onto a high-speed laser signal. GTE says that the approach can also be digital.

APOLLO-SIEMENS TIES GROW TIGHTER

Siemens AG, already Apollo Computer Inc.'s largest overseas customer with an installed base of 1,800 Apollo machines, will buy another $100 million worth of the Chelmsford, Mass., company's work stations over the next 12 months. In their latest agreement, Apollo will supply systems to Siemens's Communication and Information Systems Division. The Munich company develops work-station-based systems for applications ranging from electronic and mechanical design and computer-integrated manufacturing to technical documentation and communications.

SATELLITE SERVICE TRACKS OIL WELLS

Statistical Tabulating Corp. of Chicago is launching a computer service that will process data sent via microwaves and satellite from oil and gas wells equipped with wellhead-monitoring instrumentation. During the first year of operation, the company hopes to equip about 18,000 wells with the instrumentation, which it co-developed with Electro-Telecom Inc. of Plymouth, Mass. A computer center in Chicago will provide routine monthly account processing, as well as data analysis to assure wellhead equipment integrity and track remaining inground reserves.

CHIP BILLINGS REACH 3-YEAR HIGH

U. S. semiconductor billings reached $1.05 billion in September, a three-year high, says the Semiconductor Industry Association. September's billings were 19% higher than those in August. Bookings, however, did not match billings, causing the book-to-bill ratio for September to fall to 1.04 from 1.06 in August, notes the Cupertino, Calif., trade organization.

AMD SIGNS PACT FOR MODEM CHIP

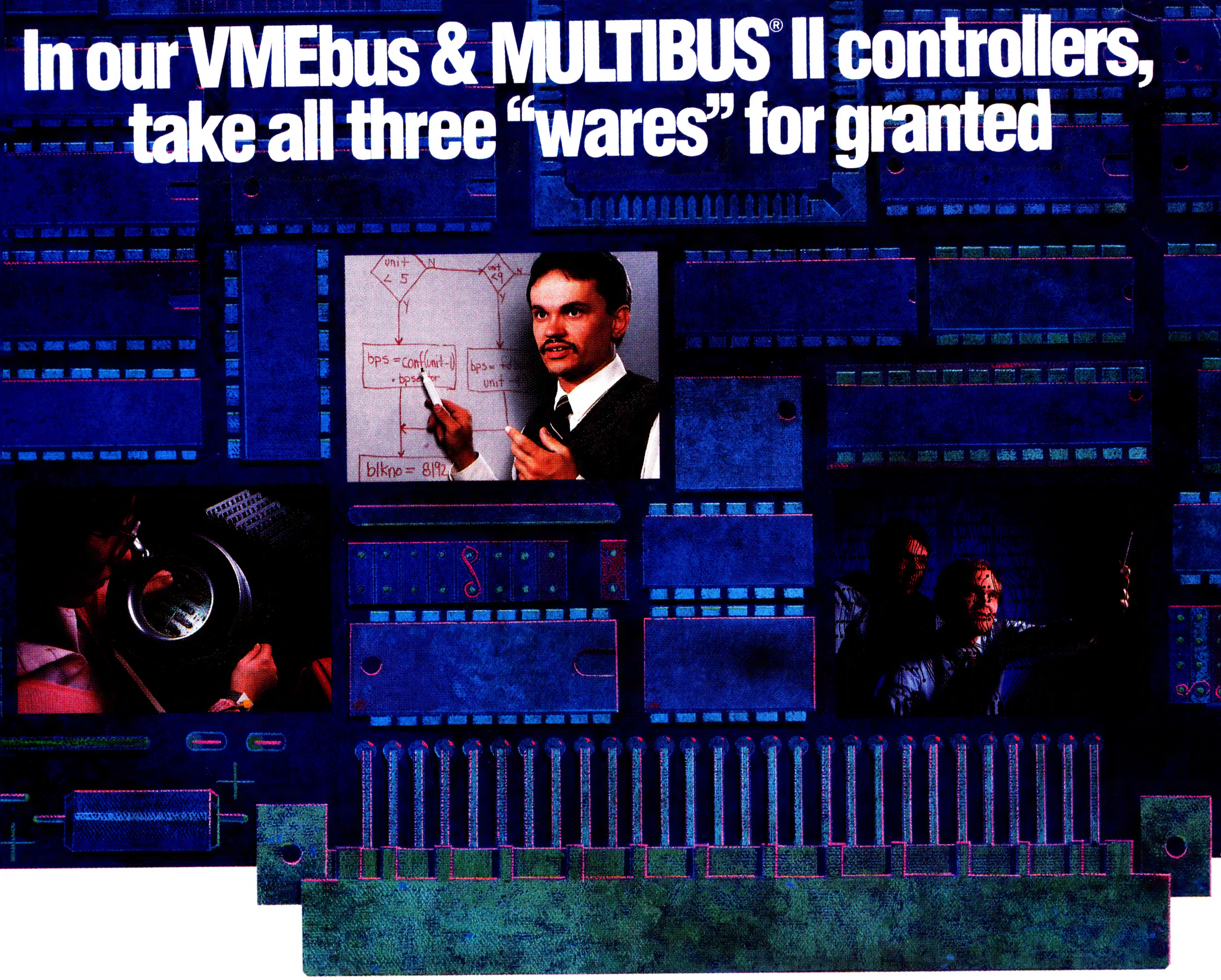
Advanced Micro Devices Inc., which dropped its plans to make its Am79C14 2,400-bit/s modem chip last year, will be introducing another chip following an agreement with Micronas in Finland. AMD and Micronas have signed a multiyear pact to cooperate in the production and marketing of telecom chips, the first of which will be the single-chip full-duplex 2,400-bit/s modem. The modem will become available in the second quarter of 1988.

SILICONIX CHOOSES MIXED ASICS

Siliconix Inc., the chip manufacturer based in Santa Clara, Calif., says it will increase the company's research and development spending in mixed analog-digital arrays and standard cells, to integrate the company's products. Steering away from the other major segment of the application-specific integrated-circuit market, Siliconix will transfer its low-voltage Si6000 and Si7000 digital gate-array families to International Microcircuits Inc., also in Santa Clara.

CO-INVENTOR OF TRANSISTOR DIES

Walter Houser Brattain, a Nobel laureate in physics who helped invent the transistor, died in Seattle, Wash., on October 13. He was 85. Brattain shared the 1956 Nobel Prize in physics with John Bardeen and William Shockley, two AT&T Bell Laboratories colleagues who helped to discover the transistor effect and develop the device in 1947.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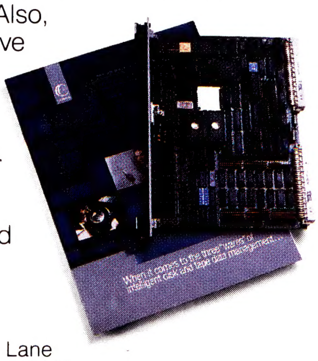

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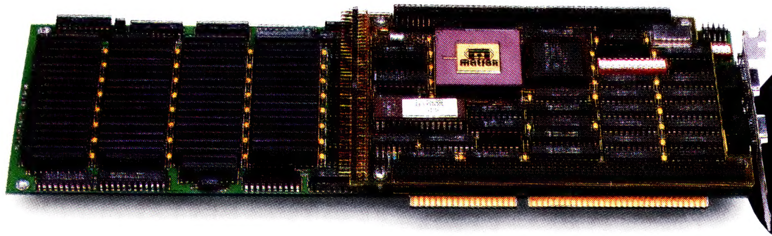

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